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Future Information Processing: From Nanodevices to Nanosystems

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Semiconductor Research Corporation

NANOARCH 2015

Boston, MA, July 8, 2015

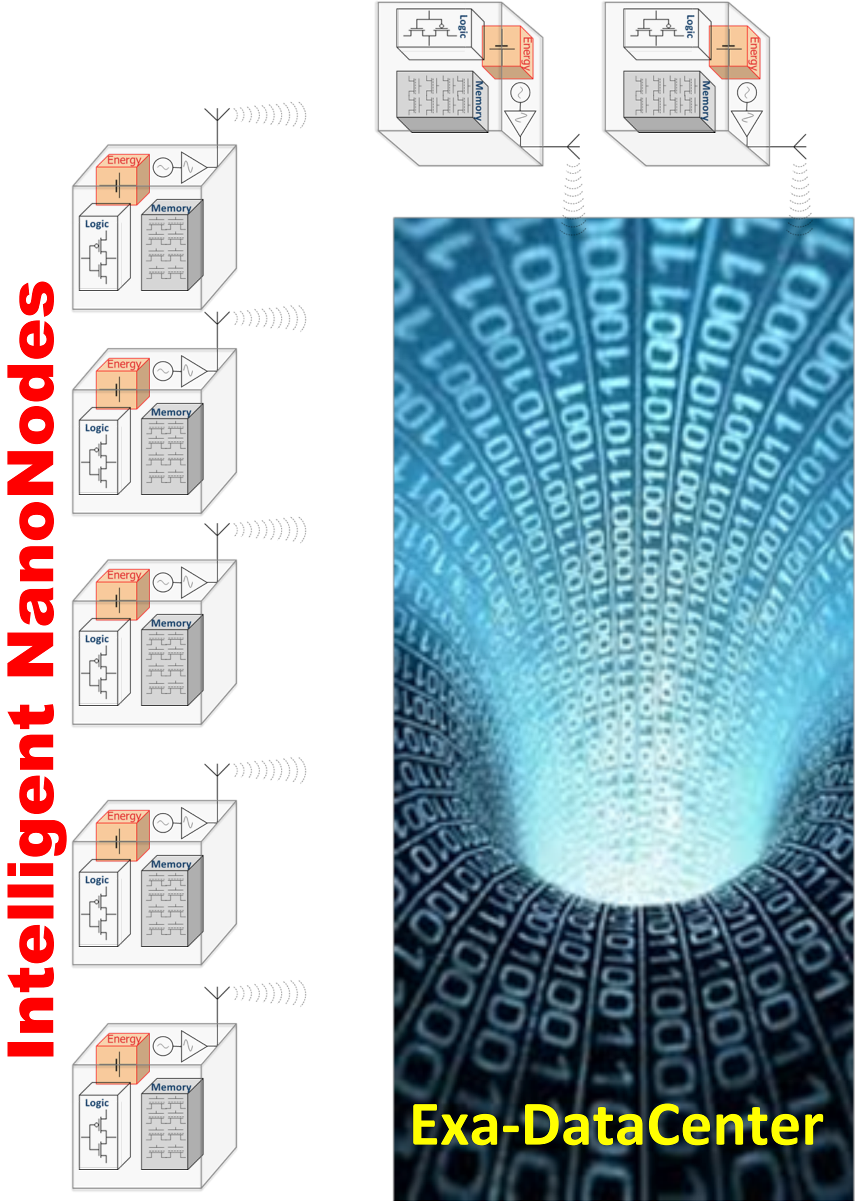
A Thought System:

Ultimate Connectivity: Internet of Nanothings

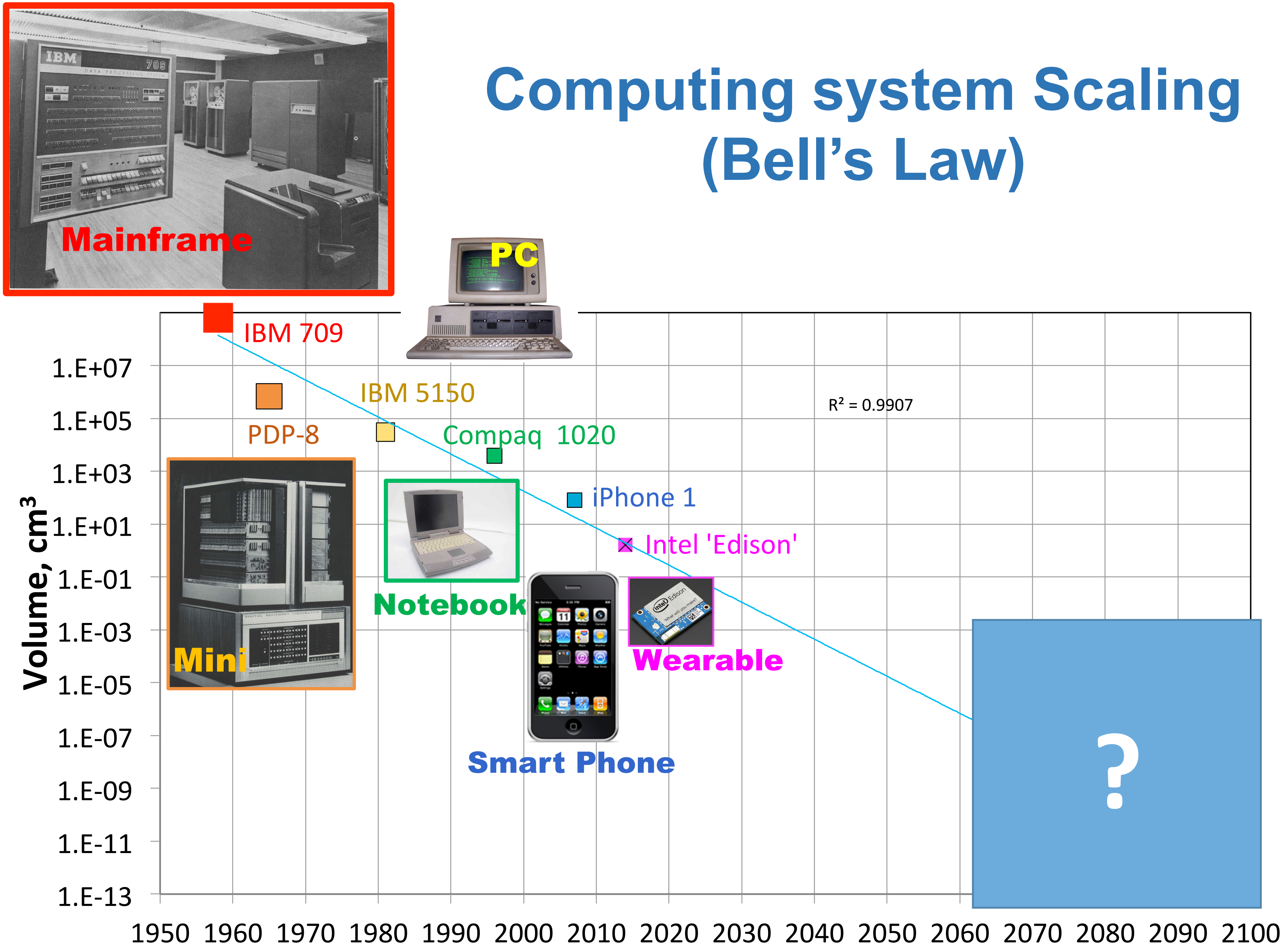
IoT Grand Challenges

I. Giga-Nano-Tera (Billions of Nanosystems connected in a THz-network)

II. Exa-DataCenters: Semiconductor Technologies for Big Data
(Radically new energy-efficient technologies for storing and analyzing massive volumes of data)

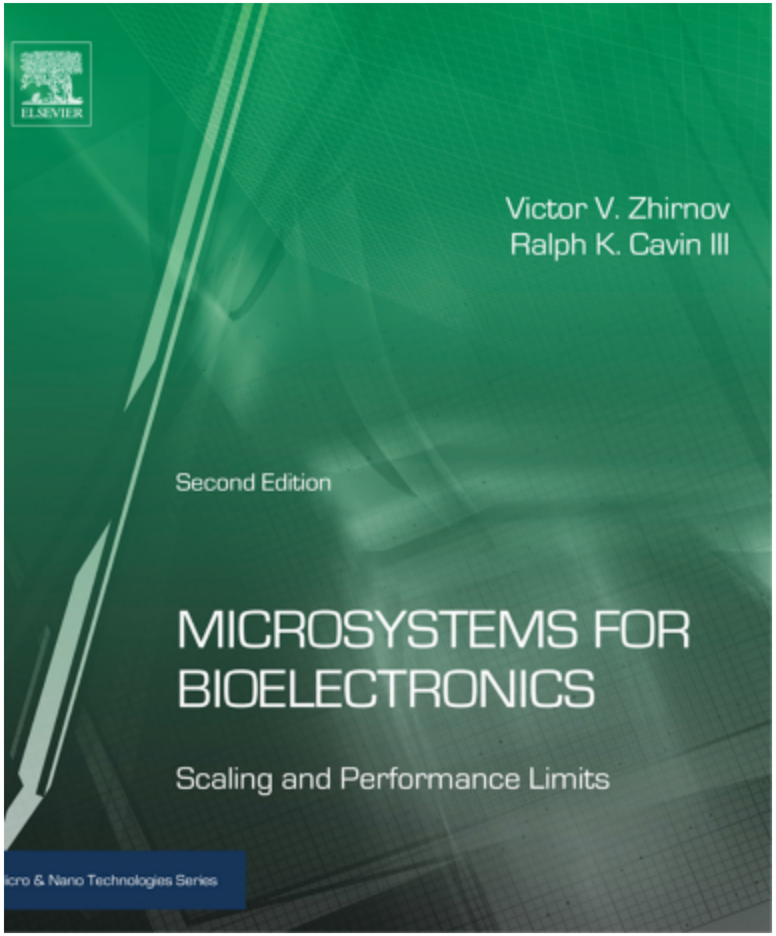


Computing system Scaling (Bell’s Law)



Outline

- Physics of extreme scaling of information processing devices and systems
- The connection of device physics and the parameters of the digital circuits
- System's "intelligence" per a volume of matter
- *In Carbo* microsystems: Design Secrets of Nature



ELSEVIER

Victor V. Zhirnov
Ralph K. Cavin III

Second Edition

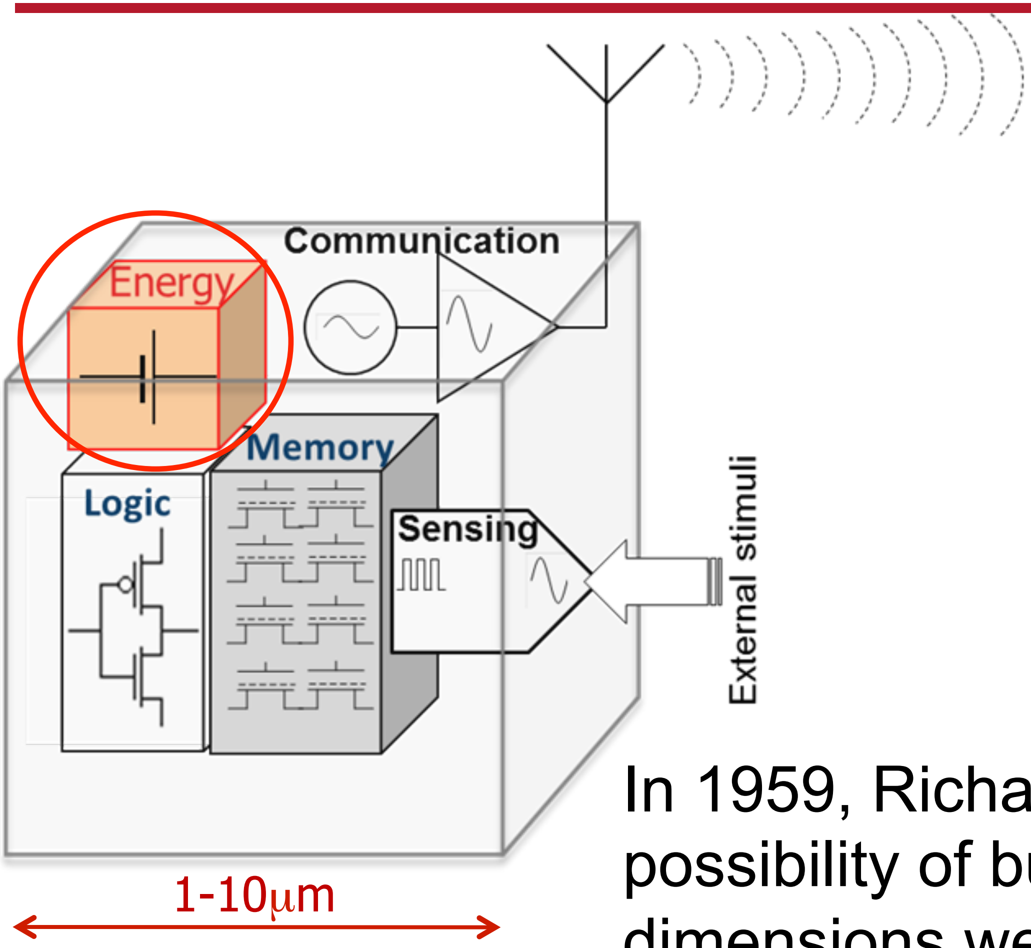
MICROSYSTEMS FOR BIOELECTRONICS

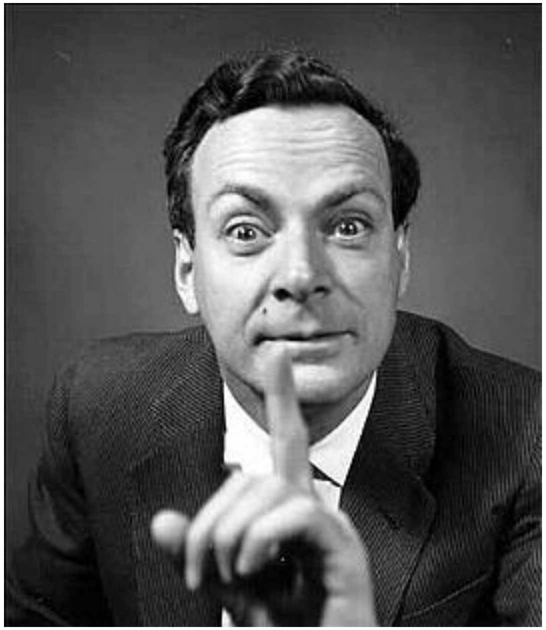
Scaling and Performance Limits

icro & Nano Technologies Series

Elsevier 2015

Miniaturizing Limits of a Computer?

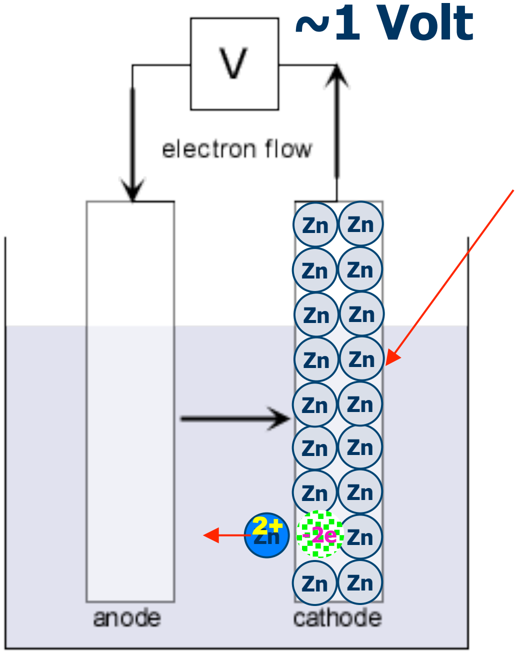




In 1959, Richard Feynman suggested the possibility of building computers whose dimensions were ‘submicroscopic’. *These submicroscopic computers remain outside of our grasp.*

Energy in the Small

Scaling limits of micro-batteries



~1 Volt

$Li \rightarrow Li^{+} + e^{-}$

$Zn \rightarrow Zn^{2+} + 2e^{-}$

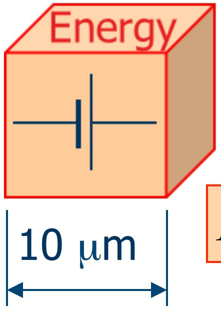
The galvanic cell consumes *atomic fuel* to produce electricity

ε~ 1eV/atom (~chemical bonding energy)

$$E = \varepsilon \cdot N$$

Number of atoms in cathode electrode

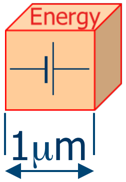
The energy output is limited by the *Avogadro's number, N_A*



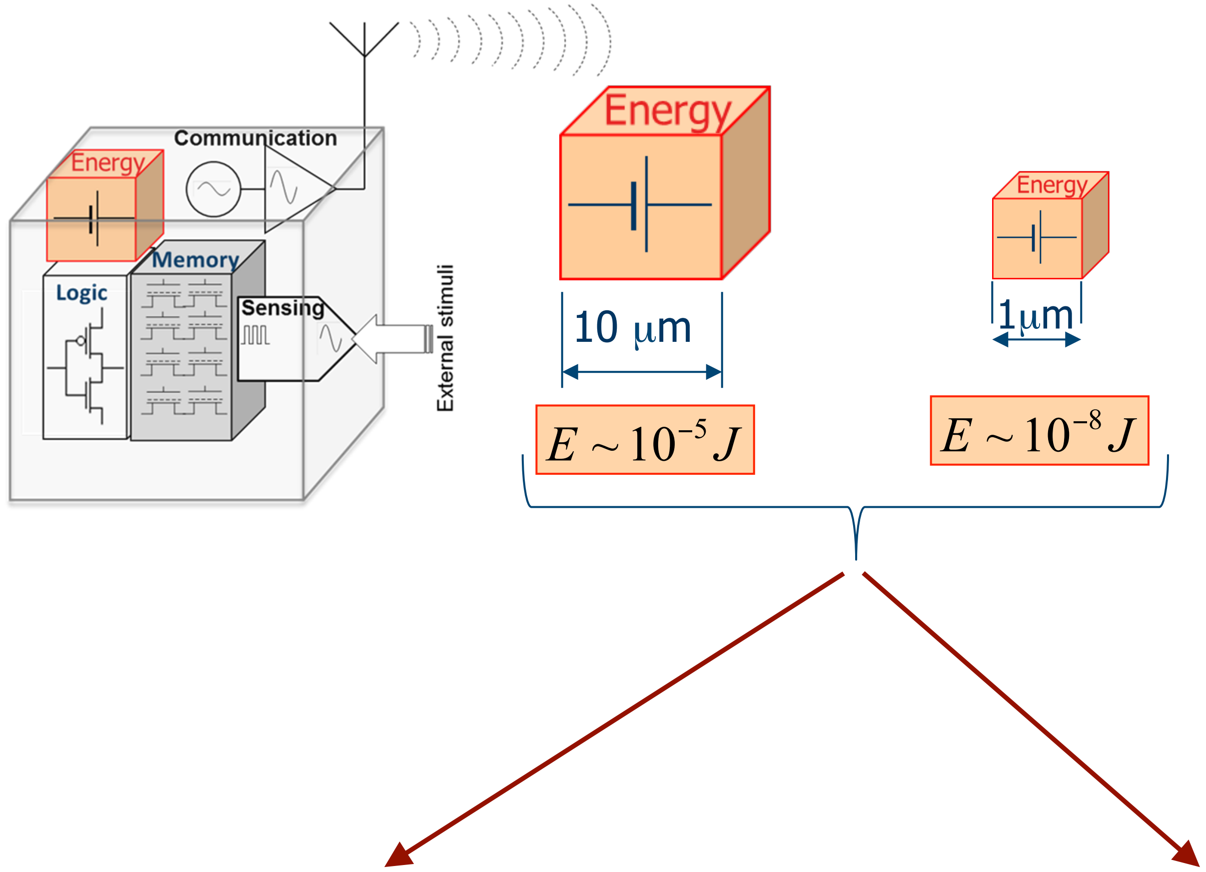
$$E_{\max} \sim eN_A \cdot 1V = 1.6\times 10^{-19} \cdot 6 \cdot 10^{23} \sim 10^{5} \frac{J}{mole} \sim 10^{4} \frac{J}{cm^{3}}$$

$$E \sim (10^{-3} cm)^{3} \cdot 10^{4} \sim 10^{-5} J$$

$$E \sim (10^{-4} cm)^{3} \cdot 10^{4} \sim 10^{-8} J$$



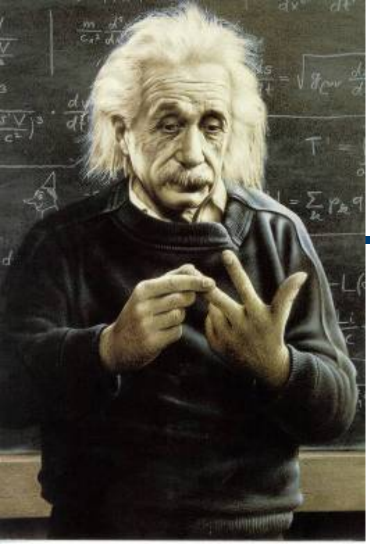
Energetics of an Autonomous Micron-Scale System Drives System Design



Communication

Computing

Wireless Communication in the Small



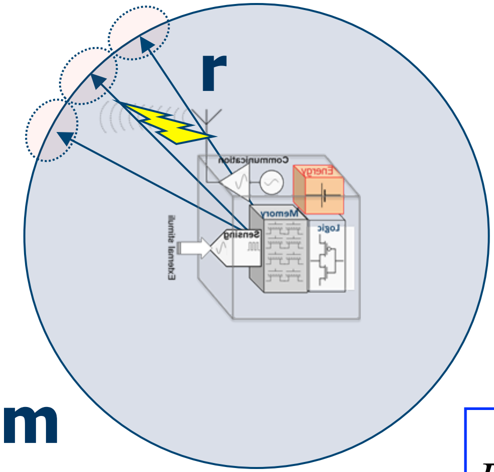
h=6.63·10^{-34} J·s

Example: Uniformly radiated wireless communication

$$E_{photon} = h\nu = \frac{hc}{\lambda}$$

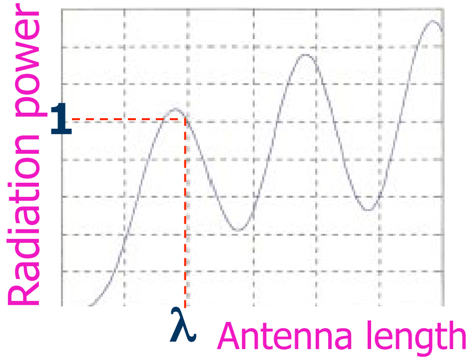
$$E_{com} = N_{photons} \cdot E_{ph}$$

$$N_{photons} \sim \frac{4\pi r^2}{\lambda^2}$$



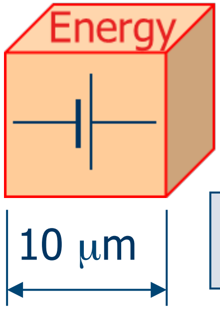
$$E_{com} \sim \frac{4\pi r^2 hc}{\lambda^3}$$

λ_{max}~10 µm



Example: r=1m

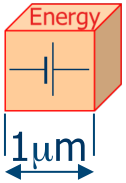
$$E_{com} = 4\pi \cdot 1^2 \cdot \frac{6.63 \cdot 10^{-34} \cdot 3 \cdot 10^8}{(10^{-5})^3} = 2.5 \cdot 10^{-9} \frac{J}{bit}$$



$E \sim 10^{-5} J$

Max number of sent bits

N_{max}=4000 bit



$E \sim 10^{-8} J$

E_{com}=2.5×10^{-6} J/bit

0 bit

Communication energy/volume expenditures is most costly activity – should therefore maximize “system intelligence”

Layers of Intelligence

1) a. Number of binary elements (Logic and Memory)
   b. Switching Speed

2) Binary Information Throughput (BIT), β

maximum number of binary transitions per unit area per unit time

bits/s

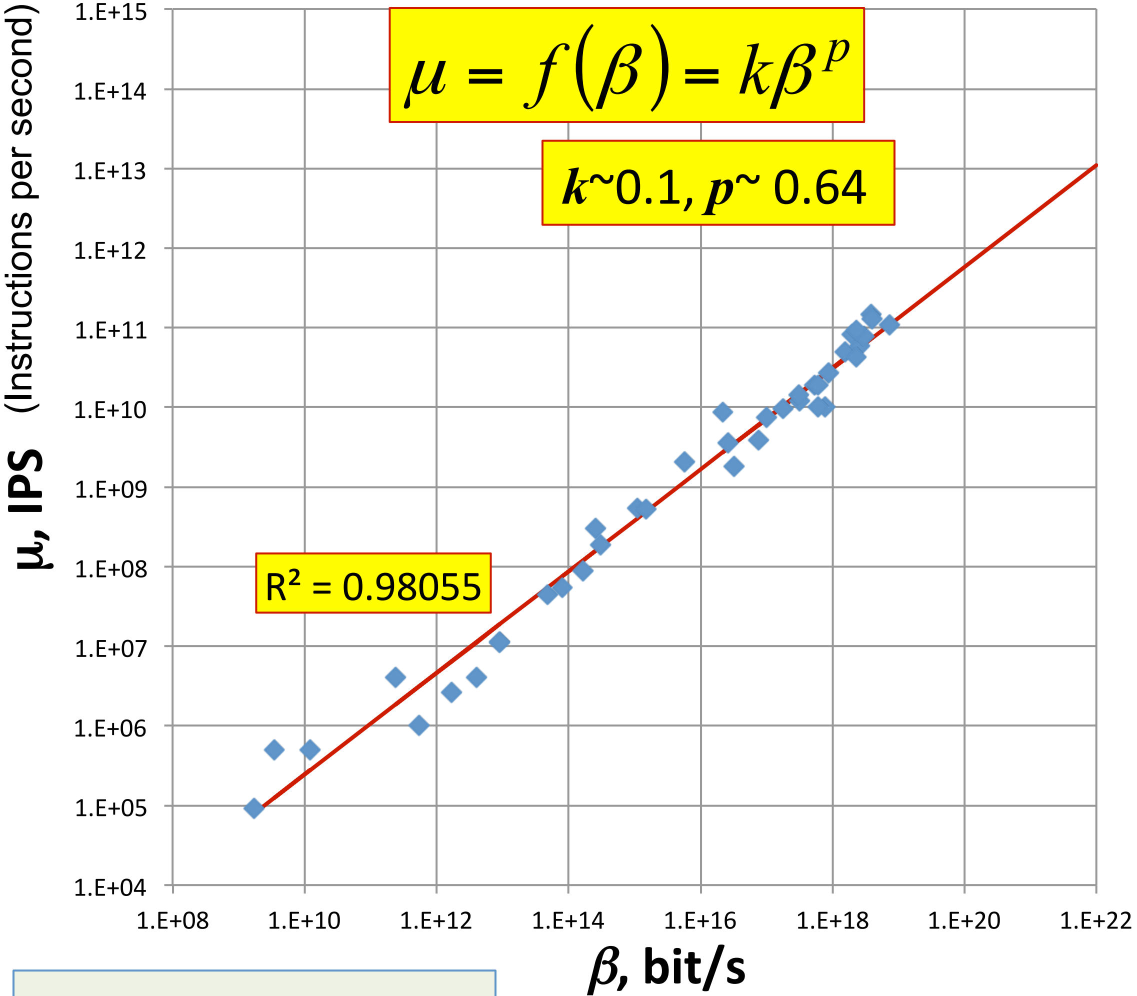
a measure of computational capability on device level

3) Algorithmic Performance, μ

MIPS, MOPS, FLOPS…

a measure of computational capability on the processor level

Benchmark capability μ (IPS) as a function of β (bit/s)



$$\mu = f(\beta) = k\beta^{p}$$

k~0.1, p~ 0.64

$R^2 = 0.98055$

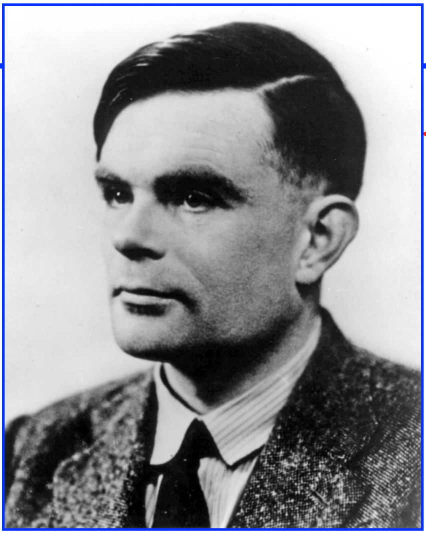
$$\beta = N_{tr} \cdot f$$

a measure of computational capability on device level

Company	Model	Year
Intel	4004	1971
Intel	8080	1974
MOS Technology	6502	1975
Motorola 68000	68000	1979
Intel	286	1982
Motorola	68020	1984
Intel	386DX	1985
ARM	ARM2	1986
Motorola	68030	1987
Motorola	68040	1990
DEC	Alpha 21064 EV4	1992
Intel	486DX	1992
Motorola	68060	1994
Intel	Pentium	1994
Intel	Pentium Pro	1996
IBM - Motorola	PowerPC 750	1997
Intel	Pentium III	1999
AMD	Athlon	2000
AMD	Athlon XP 2500+	2003
Intel	Pentium 4 Ext. Edition	2003
Centaur - VIA	VIA C7	2005
AMD	Athlon FX-57	2005
AMD	Athlon 64 3800+ X2	2005
IBM	Xbox360 "Xenon"	2005
Sony-Toshiba-IBM	PS3 Cell BE	2006
AMD	Athlon FX-60	2006
Intel	Core 2 Extreme X6800	2006
Intel	Core 2 Extreme QX6700	2006
P.A. Semi	PA6T-1682M	2007
Intel	Core 2 Extreme QX9770	2008
Intel	Core i7 920	2008
Intel	Atom N270	2008
AMD	E-350	2011
AMD	Phenom II X4 940	2009
AMD	Phenom II X6 1100T	2010
Intel	Core i7 980X	2010
Intel	Core i7 2600K	2011
Intel	Core i7 875K	2011
AMD	8150	2011

Turing-Heisenberg Rapprochement?

Instructions per second
a measure of computational capability on the processor level


Alan Turing

$$\mu = k\beta^p$$

How can we increase MIPS?

$$\beta = \frac{n_{bit}}{t_{sw}}$$

Number of binary elements

Switching time

Binary Information Throughput
a measure of computational capability on device level


Werner Heisenberg

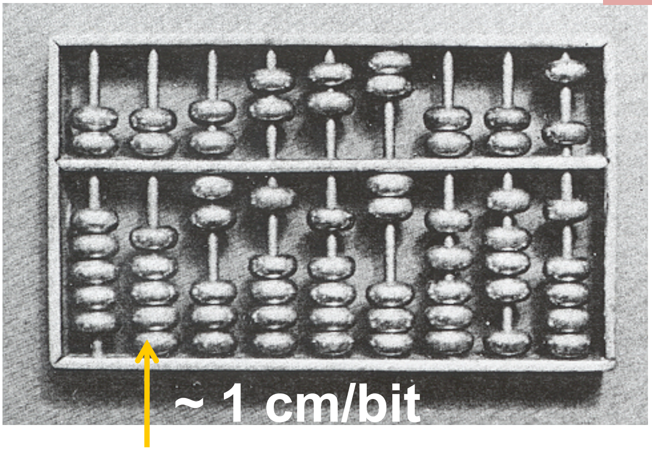

Ludwig Boltzmann

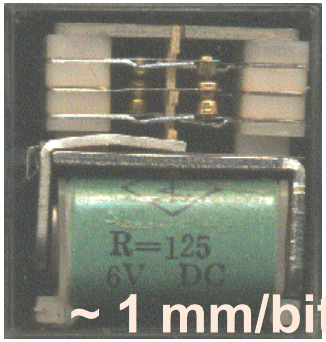
Can computational theory suggest new devices?
Stan Williams @ Nanomorphic Forum

What is Information?

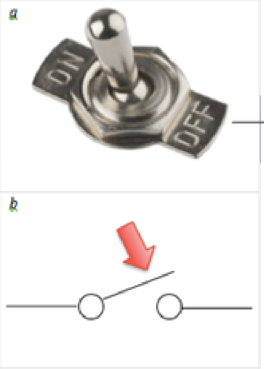
Information is measure of distinguishability

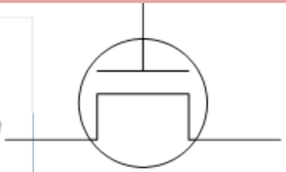
e.g. of a physical subsystem from its environment…


~ 1 cm/bit



~ 1 mm/bit





$$I = K \ln N$$

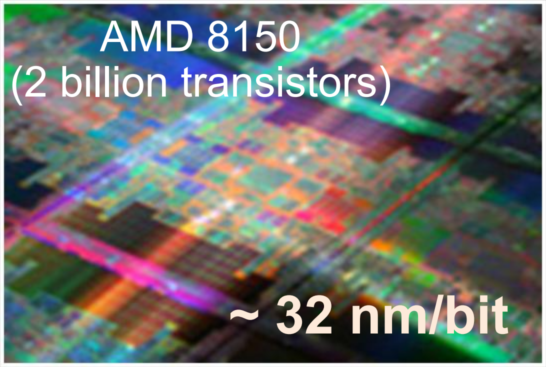
$$N_{\min} = 2$$

$$I(N_{\min}) = 1$$

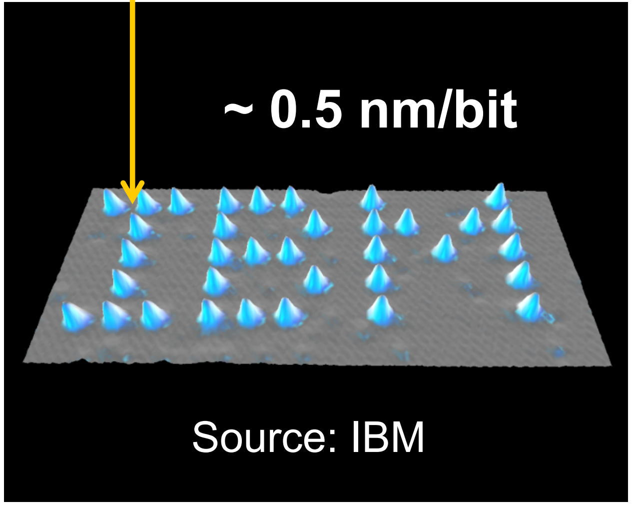
$$1 = K \ln 2$$

$$K = \frac{1}{\ln 2}$$

Information-bearing particles


AMD 8150
(2 billion transistors)

~ 32 nm/bit

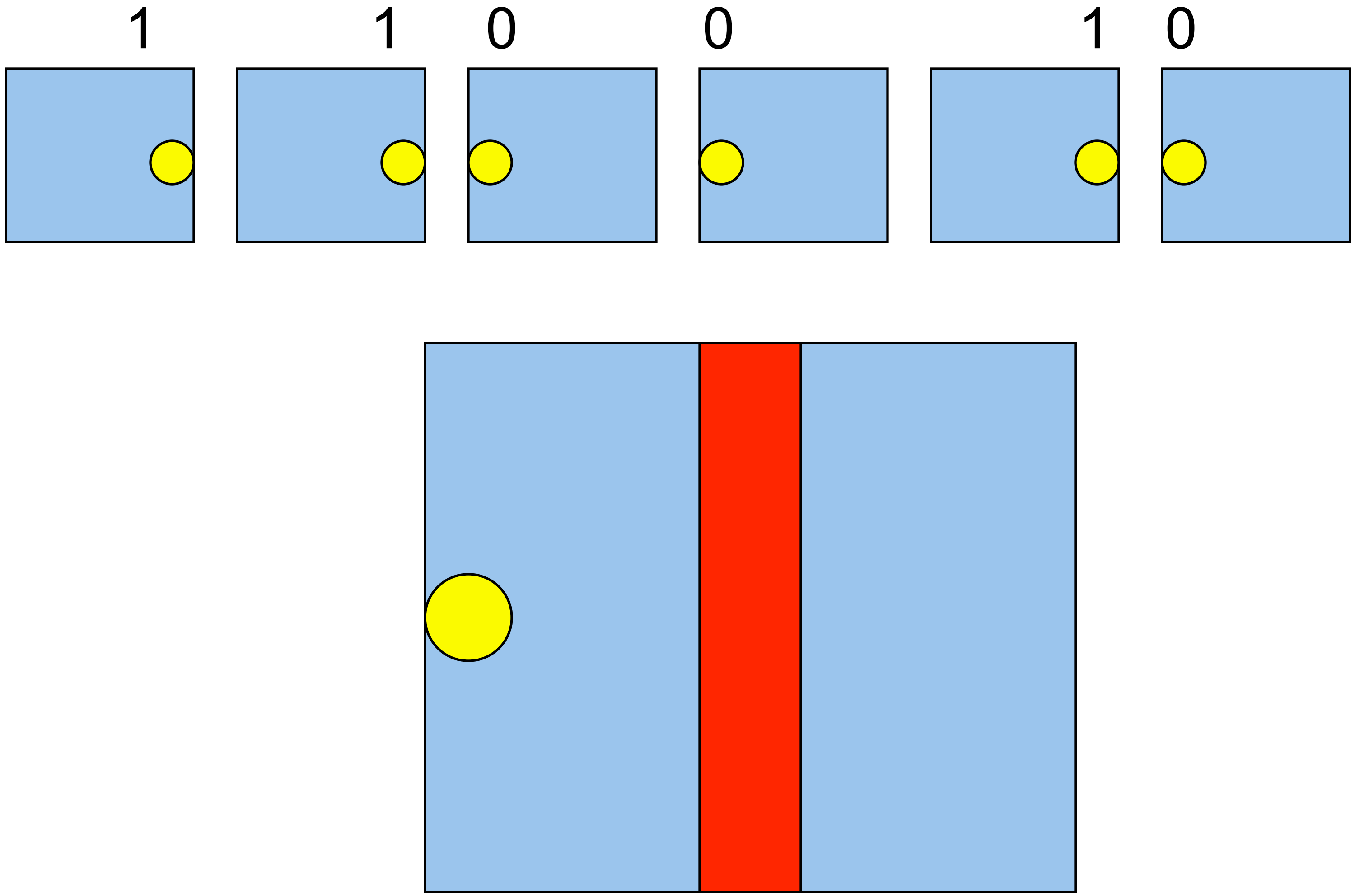

~ 0.5 nm/bit

Source: IBM

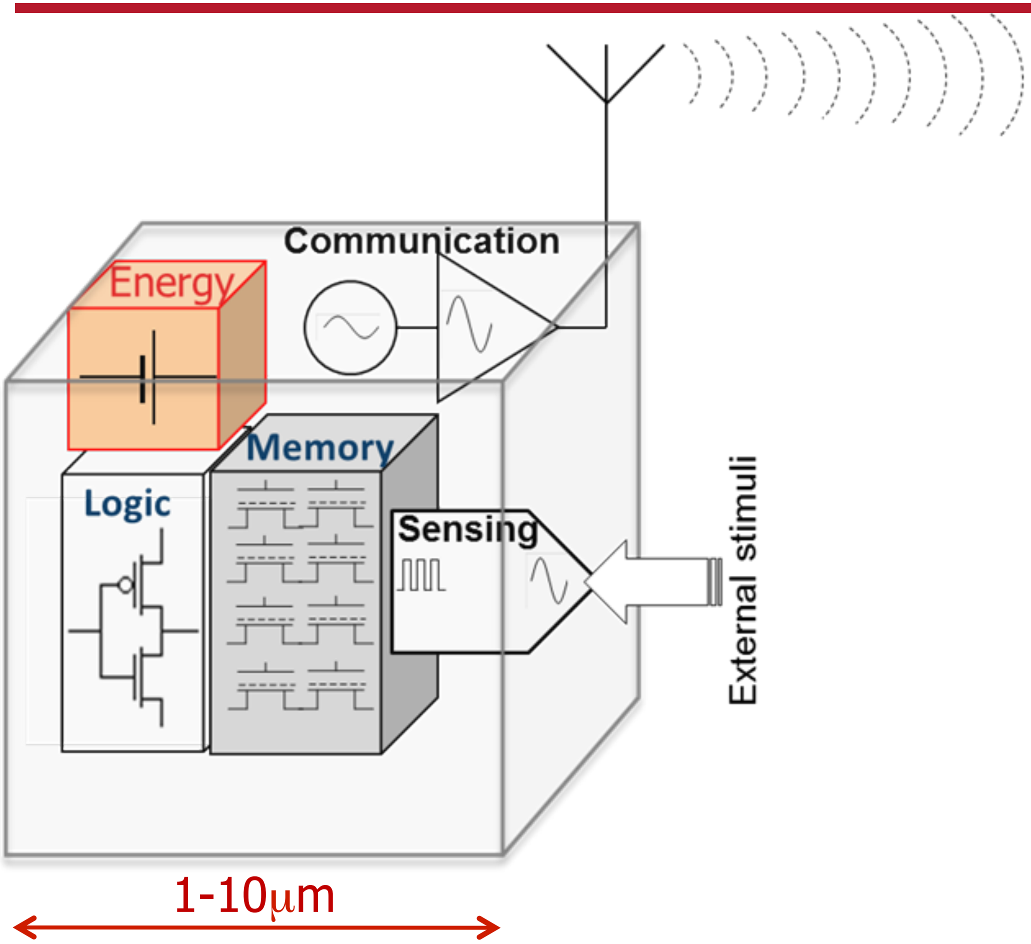
A THEME: Minimal ICT Element

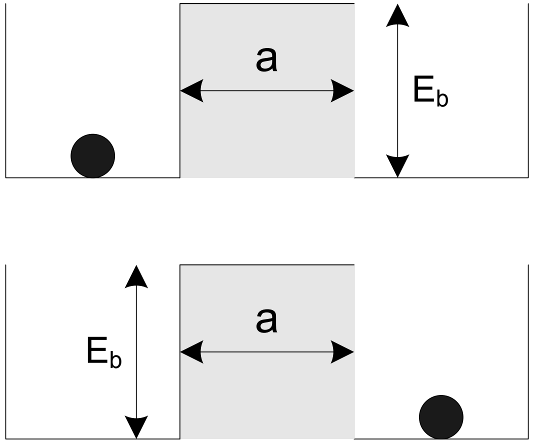
What is the smallest volume of matter needed for an ICT element? What is the smallest energy of operation?

Particle Location is an Indicator of State



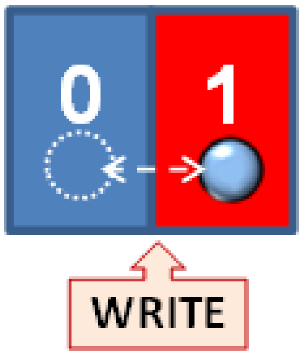
An abstract ICT-Energy element





Memory Logic Sensor

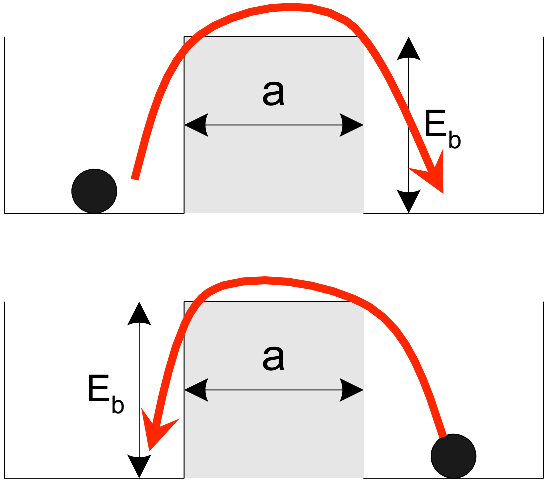
Energy



Central Concept: **Energy Barrier**

How can a barrier be created and controlled in a physical system?

Lowest Barrier:
The Boltzmann constraint



Distinguishability ***D*** implies low probability Π of spontaneous transitions between two wells (error probability)

D=max, **Π=0** ***D=0***, **Π=0.5 (50%)**

Classic distinguishability:

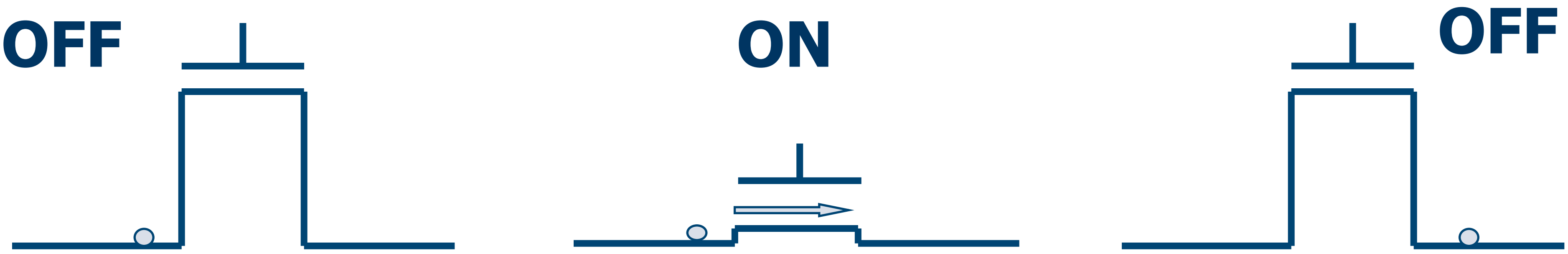
$$\boxed{\Pi_{classic} = \exp(-\frac{E_b}{k_B T})}$$

Minimum distinguishable barrier: Π=0.5

$$\frac{1}{2} = \exp(-\frac{E_b}{k_B T}) \Longrightarrow E_b = k_B T \ln 2$$

Shannon - von Neumann - Landauer limit

Switching Energy: Energy of Full-cycle



$$E_{OFF-ON} = E_b$$

$$E_{carrier}$$

$$E_{ON-OFF} = E_b$$

$$E_{bit_{\min}} = 2E_{b_{\min}} + E_{carrier}$$

$$kT\ln 2$$

We are fighting ambient thermal energy!

$$E_{SW\min} = 3k_BT\ln 2$$

x N

N – the number of electrons

$$E_{\mathrm{sw}} = 2E_{\mathrm{b}} + NE_{\mathrm{w}} = (N+2)k_BT\ln 2$$

Scaling Limits: The Heisenberg Constraint

$$E_b=k_BT\ln 2$$

Electrons in semiconductors: $m^* = 0.15 - 0.20m_0$

$\Delta p = \sqrt{2mE_b}$

$$\Delta x \Delta p \geq h$$

$$\Delta E \Delta t \geq h$$

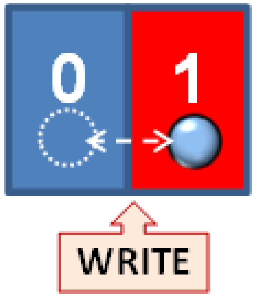
At this size, tunneling will destroy the state

$$a_{crit} \sim \frac{h}{\sqrt{2mE_b}}$$

~3-4 nm

$$t_{\min} \sim \frac{h}{E_b}$$

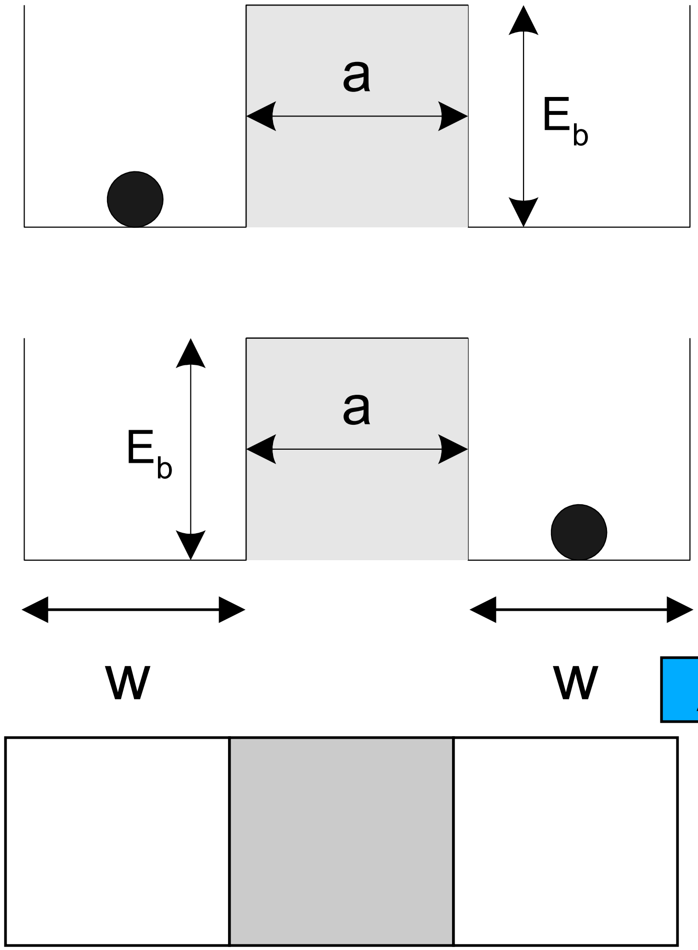
~40 fs



Minimal time of dynamical evolution of a physical system

N. Margolus and L. B. Levitin, Physica D 120 (1998) 188

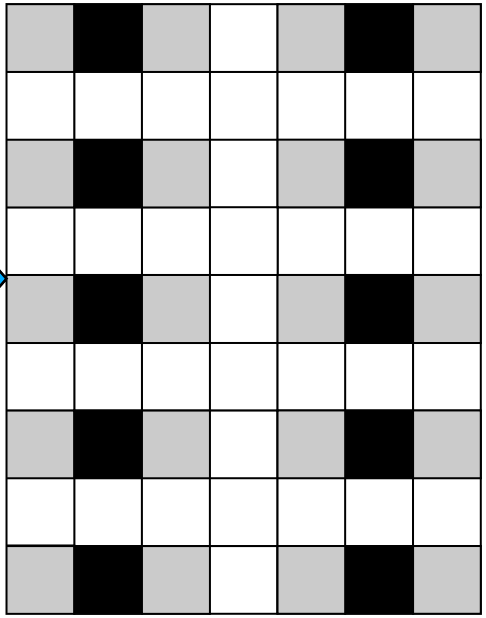
Two-well bit – Maximum areal density



Generic Floorplan
of a binary switch

Array

Joyner tiling



Device density

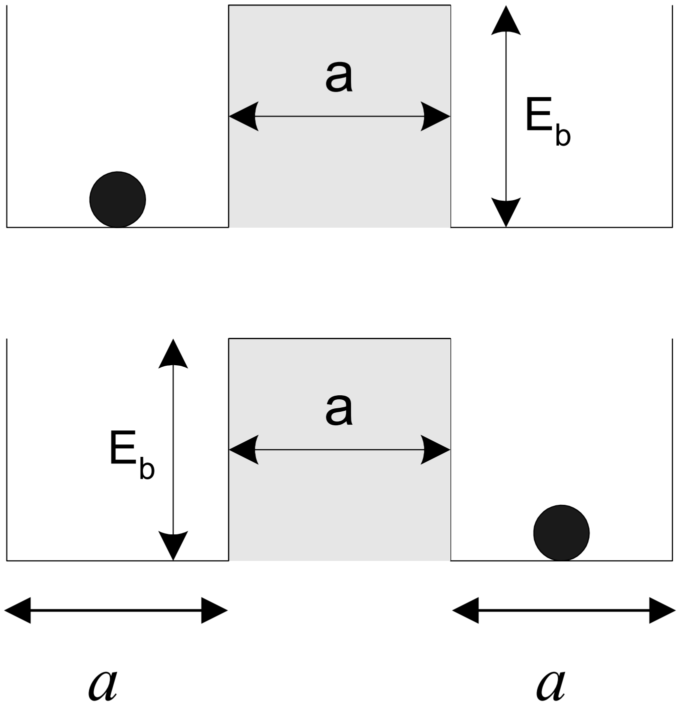
1) Upper Bound

$$n_{\max} = \frac{1}{8a^2}$$

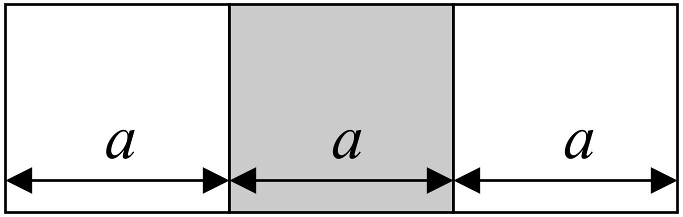
2) IC (ITRS)

$$n_{MPU} = \frac{1}{(20a)^2}$$

Binary switch abstraction:
Generic floorplan and energetics



Generic Floorplan of a binary switch



$$a = \frac{h}{\sqrt{2mkT\ln 2}} \sim 3-4nm$$

Practical limit ~5nm

$$Area_{\min} = 3a^2$$

$$E_{sw_{\min}} = 3k_BT$$

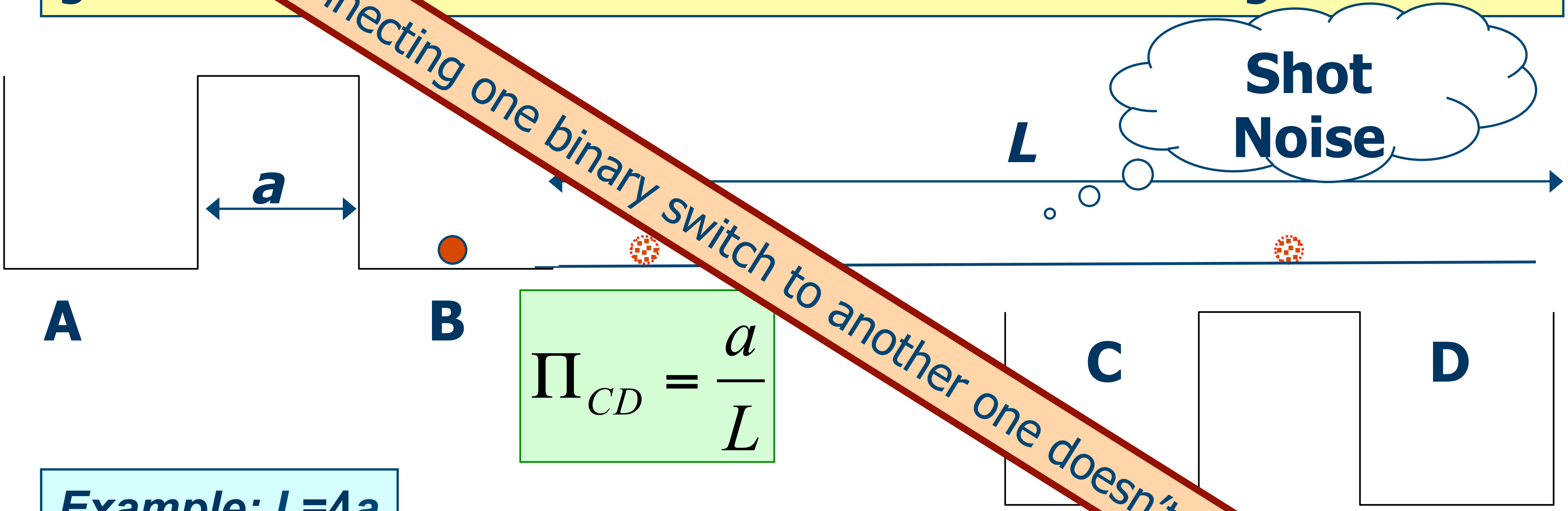
$$\varepsilon = k_BT \left(\frac{J}{tile}\right)$$

Π_{error}=0.5

Connecting Binary Switches via Wires: *Extended Well Model*

The problem is to 'place' the electron on the down stream gate – more than one electron is needed to 'charge' the line

Note: Connecting one binary switch to another one doesn't yet do computation!



$$\Pi_{CD} = \frac{a}{L}$$

Example: ***L=4a***

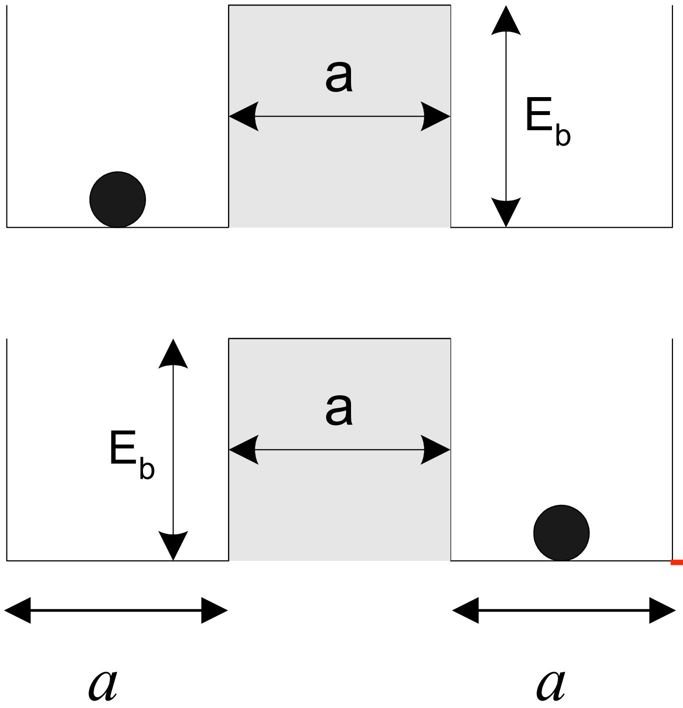
N=1→P<0.25

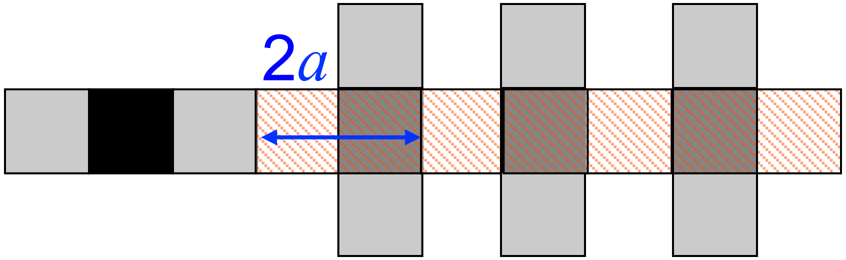
In General:

$$\Pi = 1 - \left(1 - \frac{a}{L}\right)^N$$

N – the number of electrons

Interconnect abstraction: *Extended Well Model*

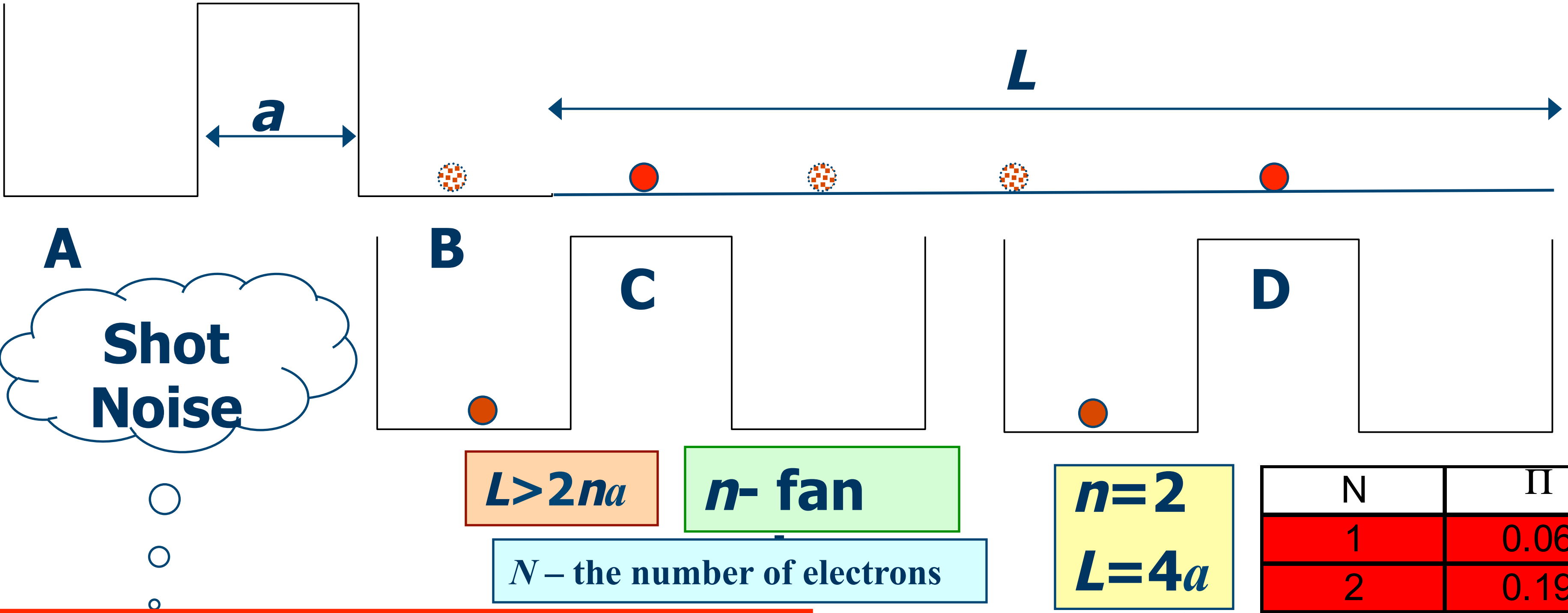




$$\boxed{L_{\min} = 2a \cdot F}$$

Connecting Binary Switches via Wires in 2D (*L>2na, N electrons*)

For logic operation, a binary switch needs to control at least two other binary switches



L>2na

***n*- fan**

N – the number of electrons

***n*=2**

L*=4*a

$$\Pi_{C\&D} = \Pi_C \times \Pi_D = \left(1-\left(1-\frac{a}{L}\right)^N\right)^2$$

N_{min}=5

N	Π
1	0.06
2	0.19
3	0.33
4	0.47
5	0.58
6	0.68

Minimum switching energy for connected binary switches

$$E_{\mathrm{sw}}=2E_{\mathrm{b}}+NE_{\mathrm{b}}=(N+2)E_{\mathrm{b}}$$

FO2

$n=2$
$L=4a$

$$N_{min}=5$$

$$E_{sw}=7k_BT\ln 2$$

FO4

$n=4$
$L=8a$

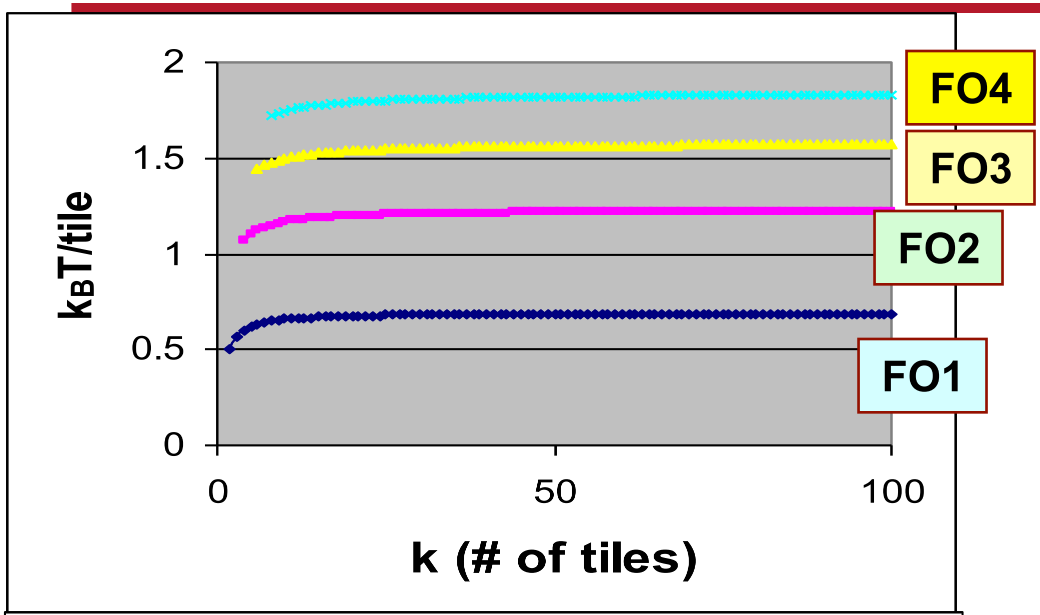
$$N_{min}=14$$

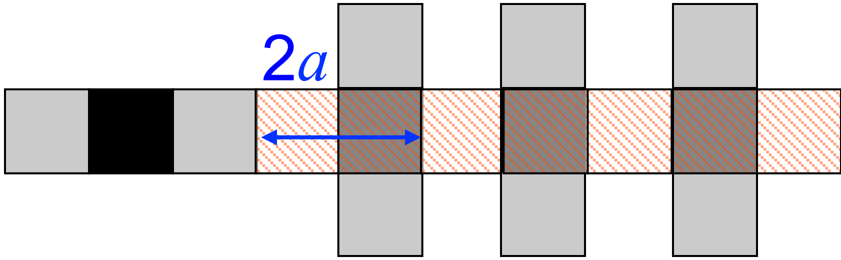
$$E_{sw}=16k_BT\ln 2$$

N	Π
1	0.00
2	0.00
3	0.01
4	0.03
5	0.06
6	0.09
7	0.14
8	0.19
9	0.24
10	0.29
11	0.35
12	0.41
13	0.46
14	0.51
15	0.56
16	0.60
17	0.65
18	0.68

Communication between logic switches takes more energy than information processing (switch operations)

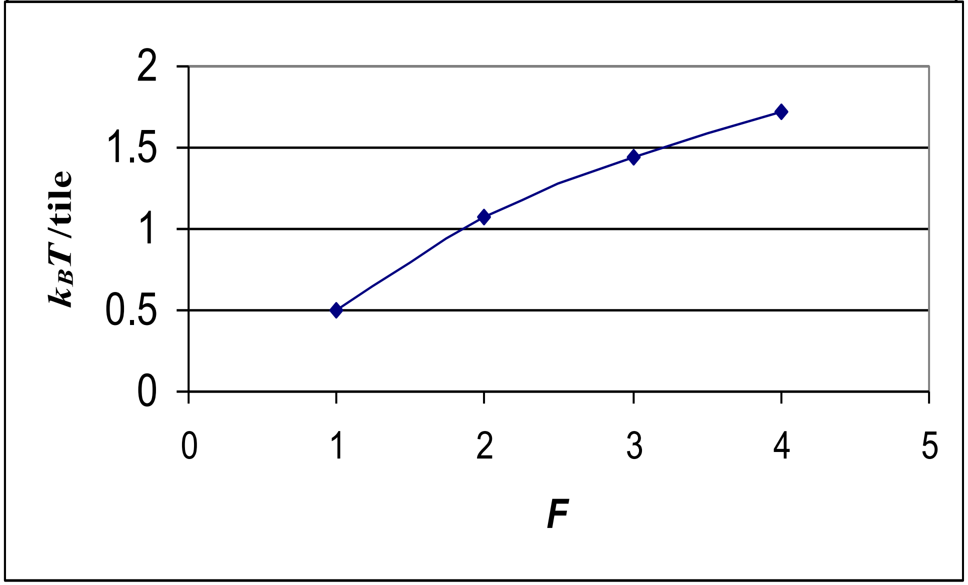
In the limits: Energy per interconnect tile





Long interconnect limit

$$\langle \varepsilon \rangle = 1.33 \ \frac{k_B T}{tile}$$



Minimum interconnect limit

$$\langle \varepsilon \rangle = 1.18 \ \frac{k_B T}{tile}$$

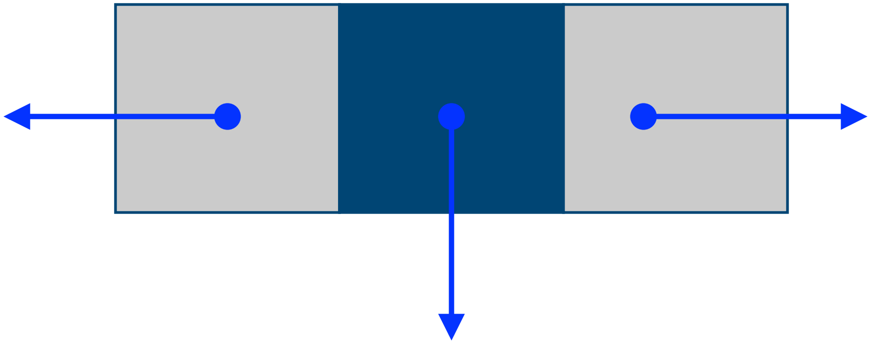
Π=0.5

$$\varepsilon \sim k_B T/\text{tile}$$

Floorspace Expenses of Communication between Binary Switches

Assumption: For each of 3 tiles of Binary Switch we need at least:

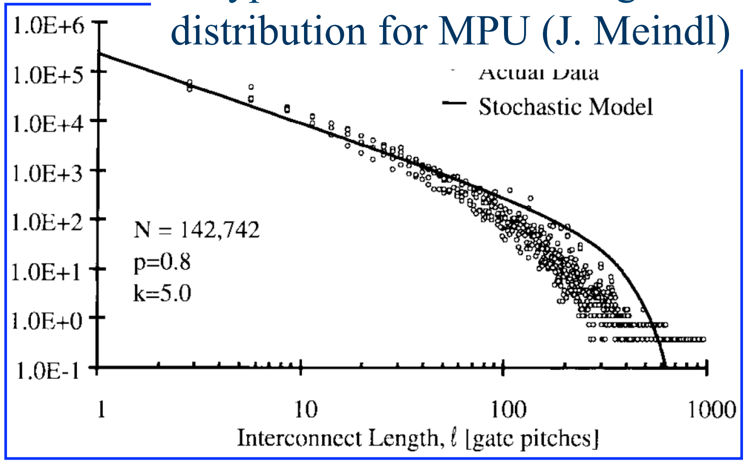
One contacting interconnect tile (3 total) and one connecting interconnect tile (3 total)



Total **6 inteconnect** tiles per binary switch

$$\boxed{L_{\text{int}} \sim 6a}$$

Reality check:

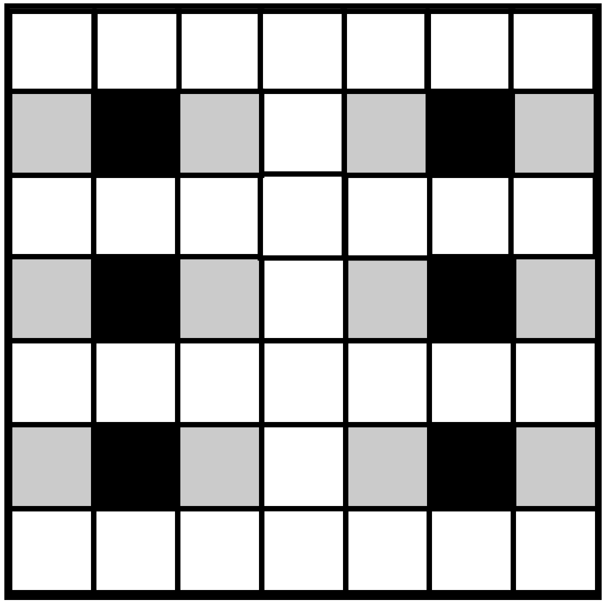


A typical interconnect length distribution for MPU (J. Meindl)

n, cm^{-2}	$\bar{L}(n)/L_g$
1.E+02	4.1
1.E+04	6.4
1.E+06	8.3
1.E+08	9.7
1.E+10	10.5

Digital circuit abstraction:
Generic floorplan and energetics and speed

Switching energy of one binary switch in a circuit



3 switch tiles

$$E_{sw}=3E_b+6E_b=9k_BT\ln 2$$

6 wire tiles

Operational energy of a circuit of *n* binary switches:

(50% activity)

$$E_{op}=\frac{9}{2}nk_BT\ln 2$$

$$Area_{\min}=n\cdot 8a^2$$

Joyner tiling

Switching delay of one binary switch in a circuit:

Speed: $\tau_{\min}$/tile

$$\tau_{\min}=\frac{\hbar}{kT\ln 2}$$

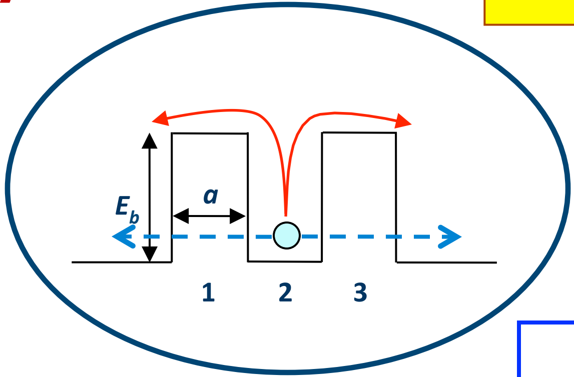
~40 fs

$$t_{sw}=9\tau_{min}$$

Minimal Electronic Memory

What is the smallest volume of matter needed for memory?

$$t_s = \frac{e}{I_s} \sim 10y$$



$$I_{o-b} = \frac{e}{h} \cdot k_B T \cdot \exp\left(-\frac{E_b}{k_B T}\right)$$

$$t_{o-b} = \frac{h}{k_B T} \exp\left(\frac{E_b}{k_B T}\right)$$

$$E_{b\min} = k_B T \ln\left(\frac{k_B T}{h} t_s\right)$$

E_{bmin}=1.3 eV

$$I_T = \frac{e}{h} \cdot k_B T \cdot \exp\left(-\frac{2\sqrt{2m}}{\hbar} \cdot a \cdot \sqrt{E_b}\right)$$

$$a_{\min} = \frac{\hbar}{2\sqrt{2mE_b}} \ln\frac{k_B T}{h} t_r$$

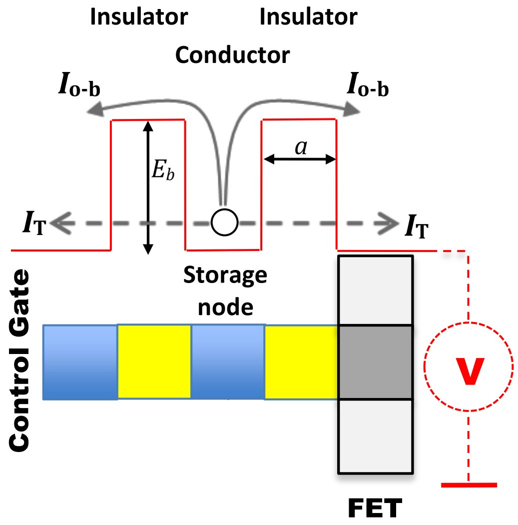
a_{min}=4.30 nm

(Limited by the mass of electron)

Adjustments: effective mass, electrostatics etc.: a_{min}~5 nm, E_{min}~2-3 eV

Electron-based Nonvolatile Memory (Flash)

1. Basic Concept

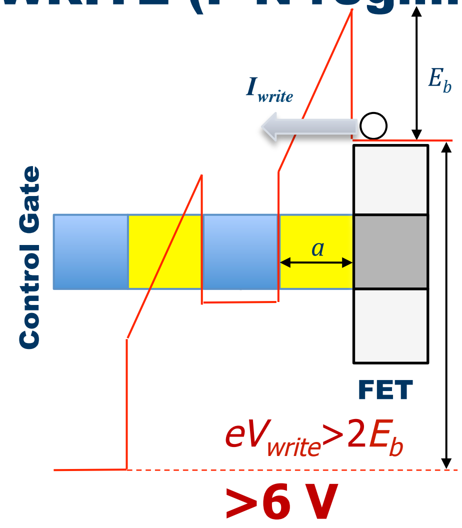


E_{bmin} >1.7 eV (>10 y retention)

$\mathbf{E_{b\,SiO2}=3.1}$ **eV**

a_{min}~5 nm

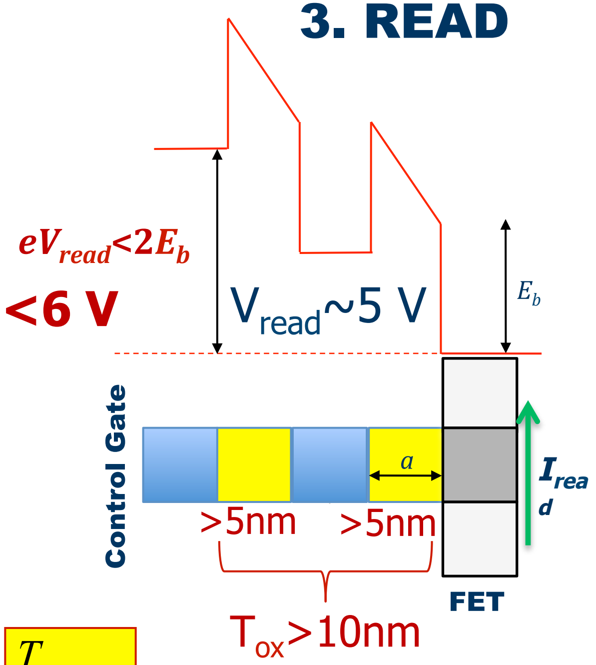
2. WRITE (F-N regime)



$V_{write\ min}$> 6-7 Volt (very slow)

V_{write} >**10-15 Volt** (ms-µs)

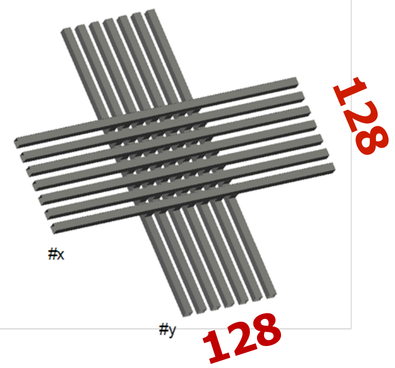
3. READ



$$\frac{T_{ox}}{L_{ch}} \sim 1$$

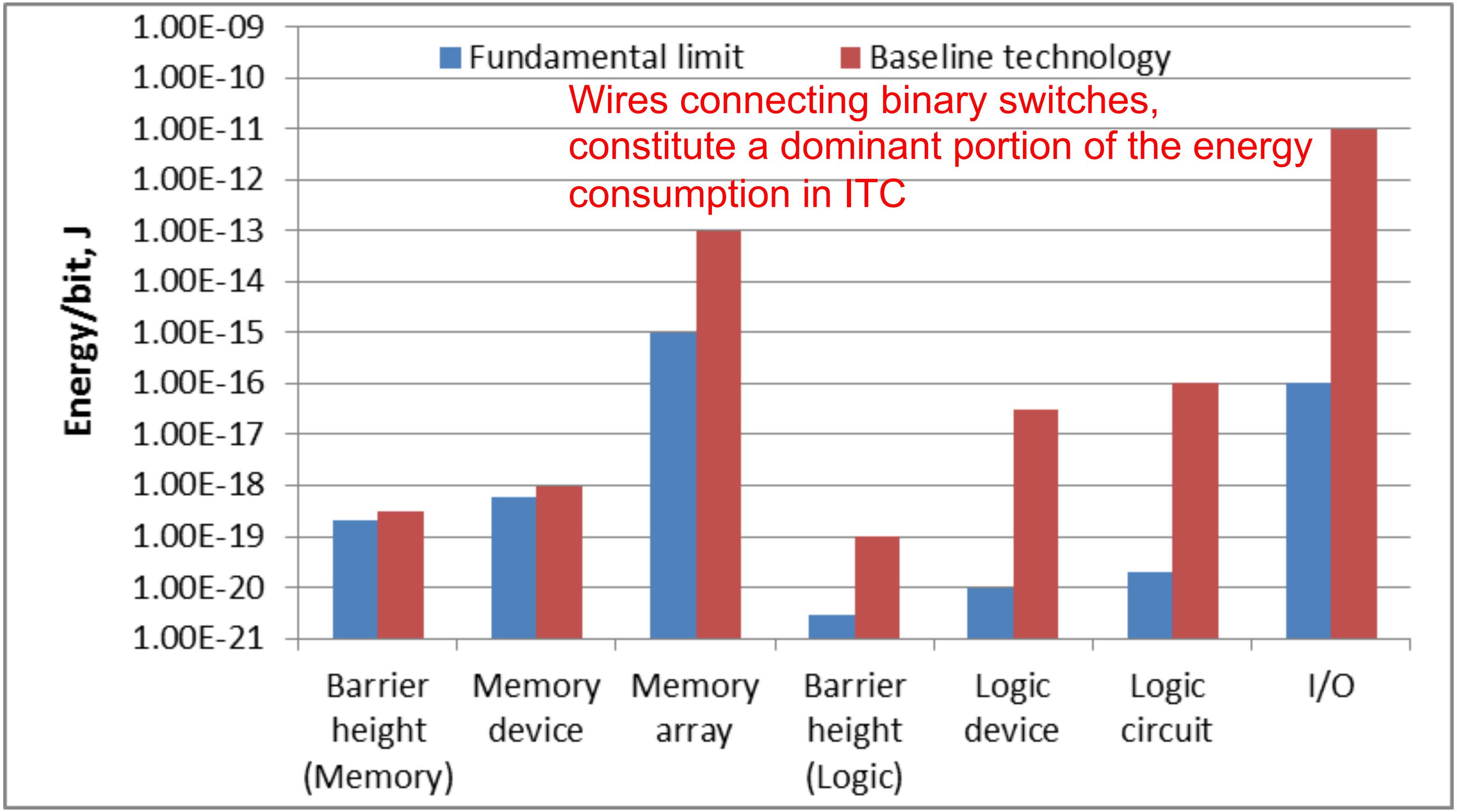
$F_{min}>10nm$

4. Array



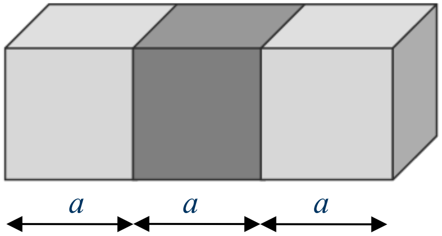
$$E_M \sim C_{line}V^2 \sim 10^{-14}J$$

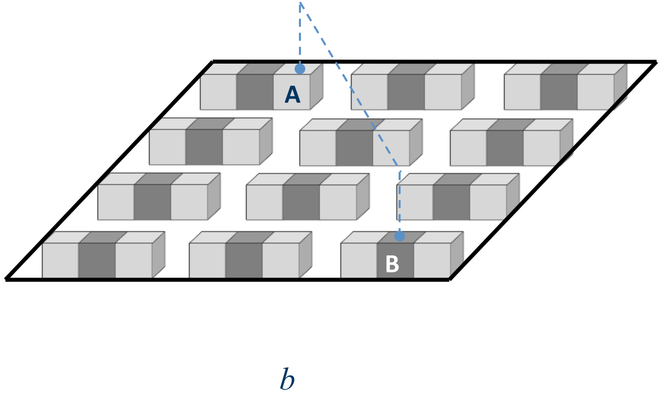
Charge based computing: A Summary


Wires connecting binary switches, constitute a dominant portion of the energy consumption in ITC

Minimal 3D Electronic Logic Switch: Volume bounds

3D tiling

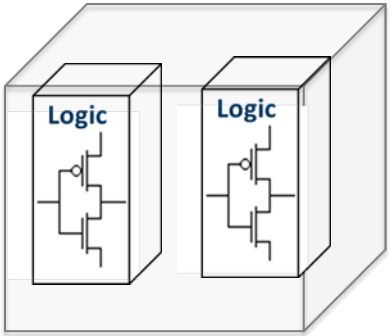




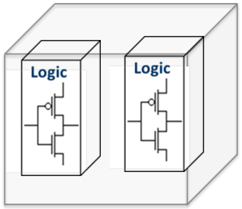
a_{min}~5 nm

(Limited by the mass of electron)

$$n_{3D} \sim= \frac{1}{96a^3} \sim 8\cdot10^{16}\,\frac{bit}{cm^3}$$



$N_{tr}=8\times10^7$ 10 μm

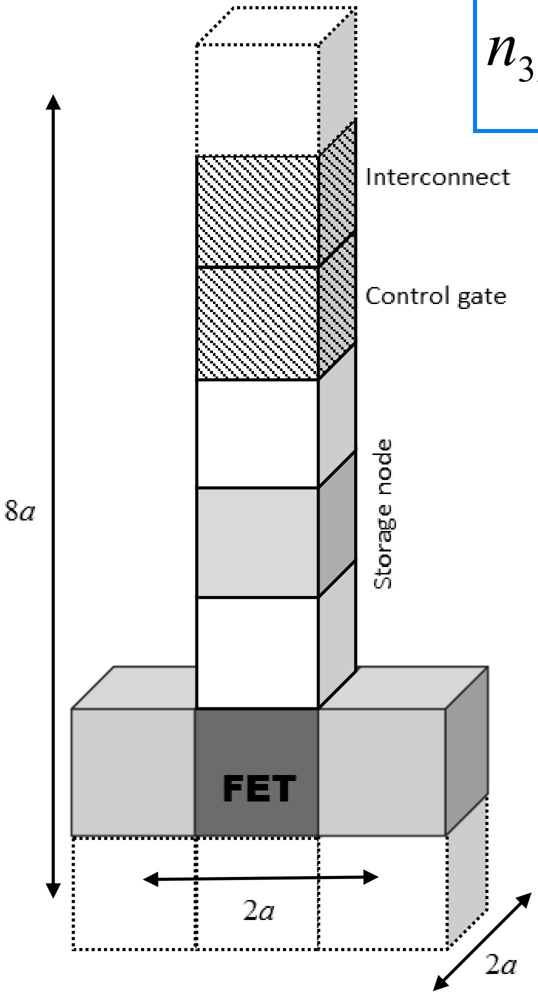


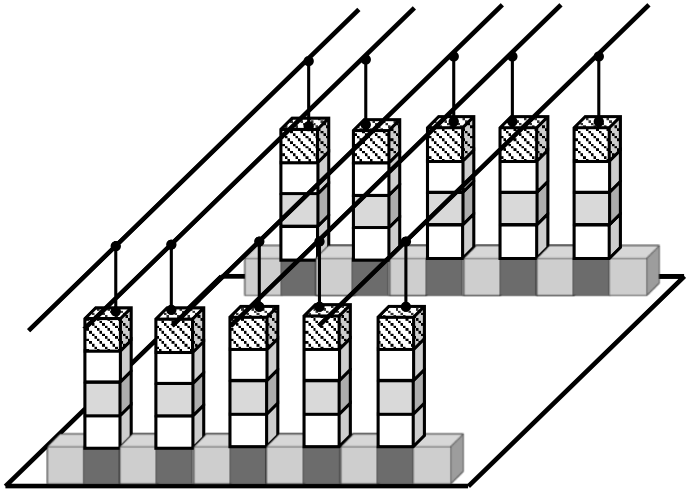
$N_{tr}=8\times10^4$

1μm

Minimal Electronic Memory: Volume bounds

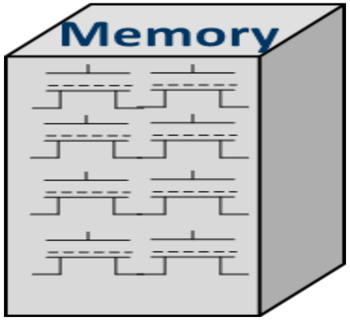
$$n_{3D} \sim \frac{1}{32a^3} \sim 10^{17}\,\frac{bit}{cm^3}$$





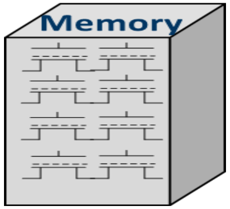
a_{min}~5 nm

(Limited by the mass of electron)



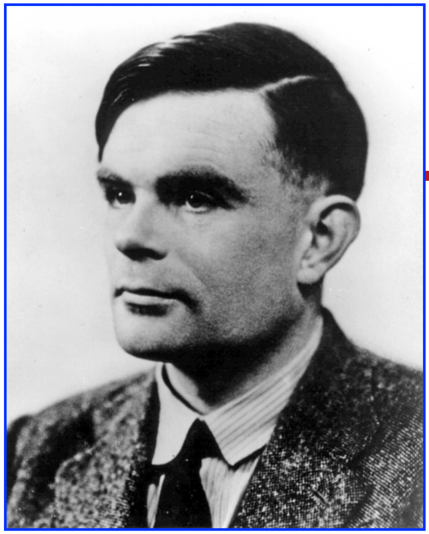
10 μm

N~100 Mbit

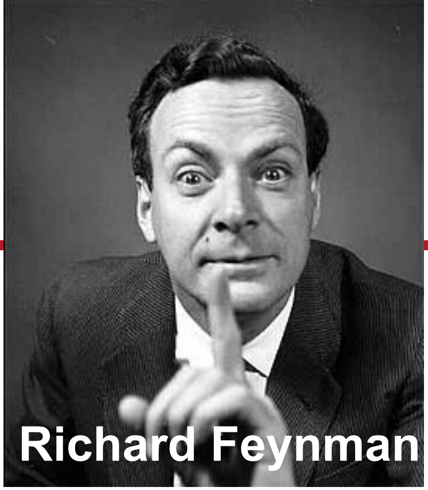


1 μm

N~100 kbit



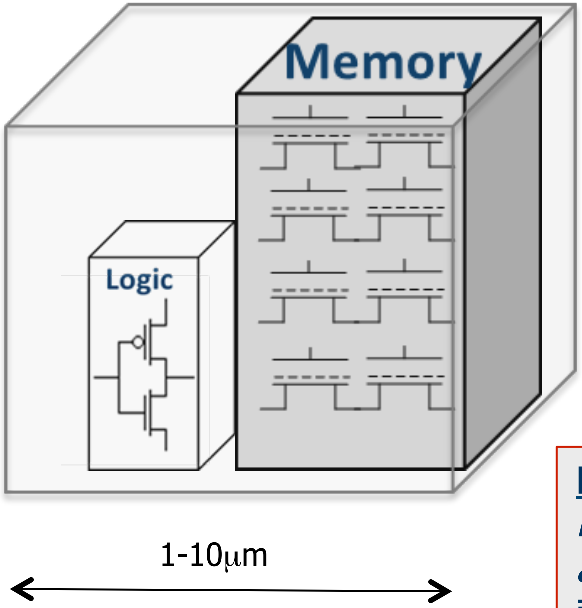
Miniaturizing Limits of a Computer?



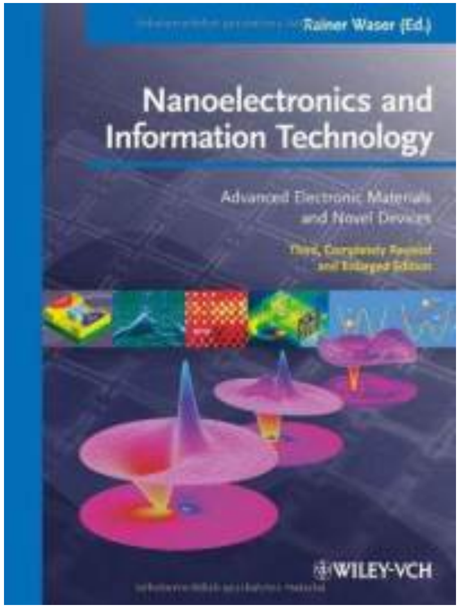
Richard Feynman

Turing Machine

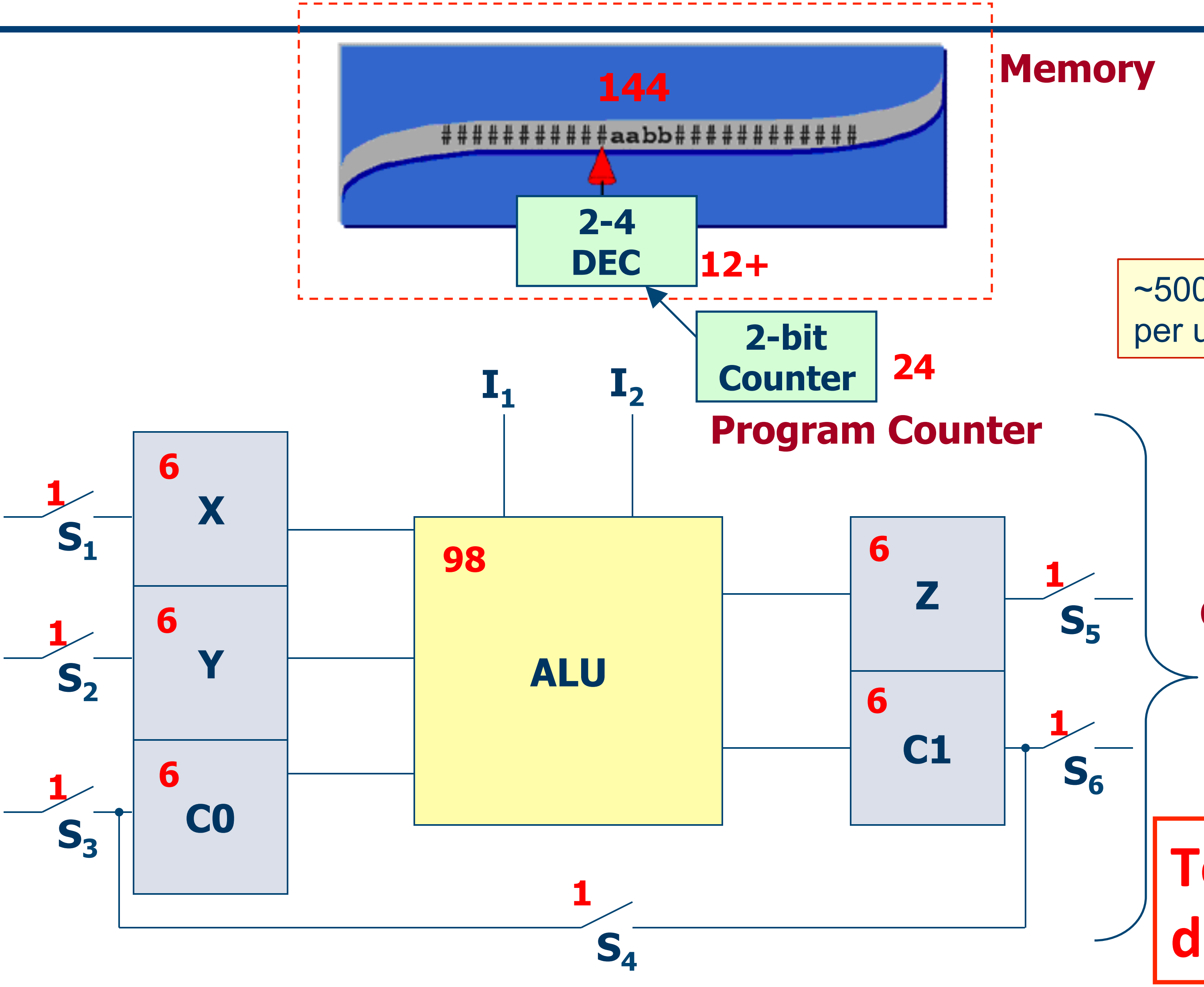
A complete ‘computer’ must contain both logic unit and ‘tape’ (nonvolatile memory)

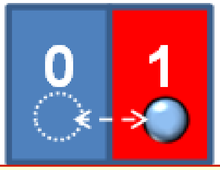


R. Cavin, W. Joyner, and T. Noll, **Chapter 22**: *Performance Estimates for Microprocessors: at Technology Limits and in Practice*, in: **Nanoelectronics and Information Technology,** by R. Waser (Ed.) (Wiley 2012)



Minimal Turing Machine

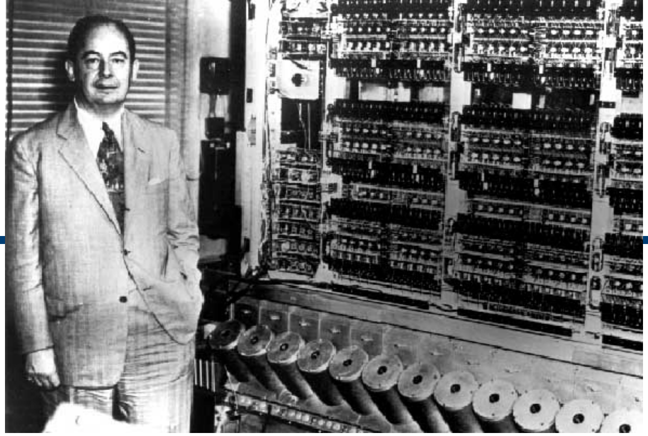




~500 “raw” bit transitions per useful bit

Total: 320 devices

Von Neumann's Threshold



John von Neumann:

If one constructs the automaton (A) correctly, then any additional requirements about the automaton can be handled by sufficiently elaborated instructions. This is only true if A is sufficiently complicated, if it has reached a certain minimum of complexity

Von Neumann's estimate: N_{min}~a few hundred switches

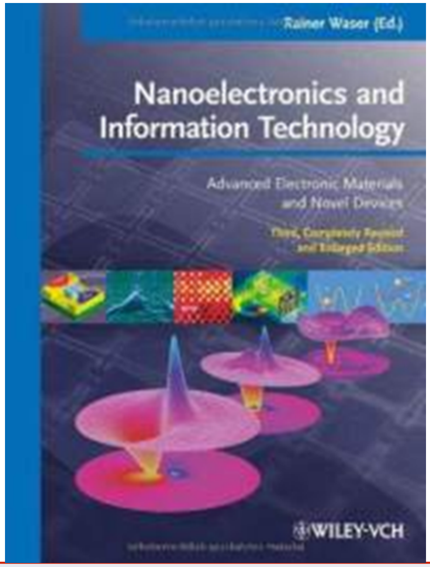
(J. von Neumann, The Computer and the Brain. Yale Univ. Press, 1959)

Cavin-Joyner-Noll abstraction (CJN):

In an attempt for a more accurate estimate of the von Neumann threshold, a model 1-bit Minimal Turing Machine (MTM) has been constructed

MTM Essentials:

Total device count:	**320**
Instruction word length:	**8-bit**
Cycles per output bit:	**3**
"Raw" bits processed per output bit:	**~500**



R. Cavin, W. Joyner, and T. Noll, **Chapter 22**: *Performance Estimates for Microprocessors: at Technology Limits and in Practice*, in: **Nanoelectronics and Information Technology,** by R. Waser (Ed.) (Wiley 2012)

Si-μCell: A hypothetical 1μm³ Si computer

Logic

N_{tr}= 320,

$E_b=6k_BT$ ($\Pi_{syst}=0.5$)

$E_{sw}=54k_BT$

$E_{cycle} = 8640k_BT=3.6\times10^{-17}$ J/cycle

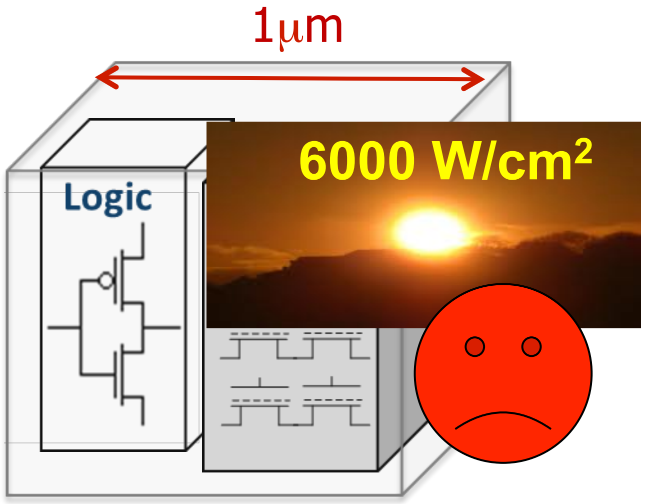
$t_{cycle}\sim16$ps

Memory

N=100 kbit

$E_M\sim 10^{-14}$ J

$$P=\frac{E_L+E_M}{t_{cycle}}\sim\frac{3.6\cdot10^{-17}+10^{-14}J}{16ps}=6.27\cdot10^{-4}W=627\mu W$$



$$\frac{P}{A_{1\mu m}}=\frac{627\mu W}{6\cdot(1\mu m)^2}=10540\frac{W}{cm^2}$$

Must slow down!

Exceeds capability of known cooling techniques

Heat-constrained operation

	Heat transfer coefficient, W/(cm^2·K)	Heat flux, W/(cm^2)
Cooling techniques		
Free convection, air	$(5\text{-}25)\times10^{-4}$	0.05-0.25 ($\Delta T=100$K)
Free convection, water	$(20\text{-}100)\times10^{-4}$	0.2-1 ($\Delta T=100$K)
Forced convection, air	$(10\text{-}500)\times10^{-4}$	0.1-5 ($\Delta T=100$K)
Forced convection, water	$(100\text{-}15{,}000)\times10^{-4}$	1-150 ($\Delta T=100$K)
Reference examples		
Human body	–	0.01
Hot plate	–	10
Microprocessor chip	–	20-60
Sun's surface	–	6000

No overheads

Space and energy overheads

If it is postulated that only passive cooling can be used for the *Si-μCell*, the maximum heat flux through the walls of the cube must be **<1W/cm^2**.

total power **<6×10^{-8} W**
cycle time **>170ns.**

Si-μCell: A hypothetical 1μm^3 Si computer

Logic

N_{tr}= 320,

E_b=6k_BT (Π_{syst}=0.5)

E_{sw}=54k_BT

E_{cycle} = 8640k_BT=3.6×10^{-17} J/cycle

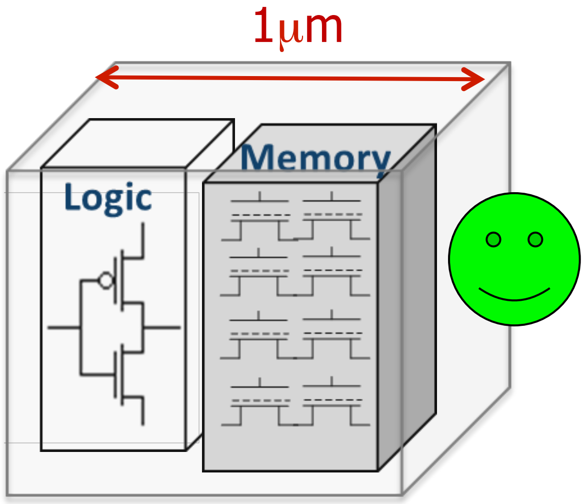
t_{cycle}~170ns

Memory

N=100 kbit

E_M ~ 10^{-14} J

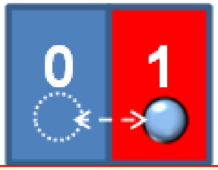
$$\boxed{P = \frac{E_L + E_M}{t_{cycle}} \sim \frac{3.6\cdot 10^{-17} + 10^{-14} J}{170ns} = 6\cdot 10^{-8} W = 60nW}$$



$$\frac{P}{A_{1\mu m}} = \frac{60nW}{6\cdot(1\mu m)^2} = 1\frac{W}{cm^2}$$

System's "intelligence" per a volume of matter

Si-μCell: A hypothetical 1μm³ Si computer



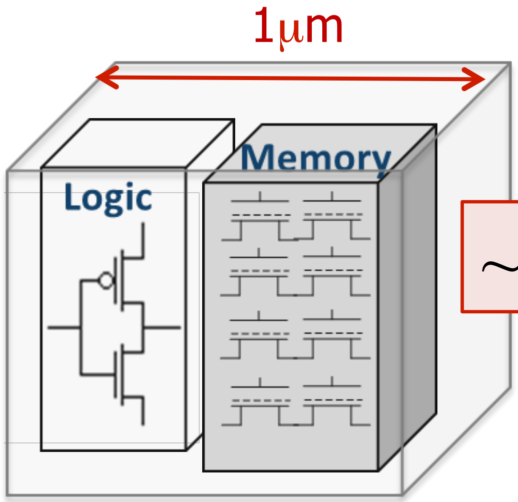
a_{min} ~ 5 nm

Logic

$$n_{3D} \sim 8 \cdot 10^{16} \frac{bit}{cm^3}$$

Memory

$$n_{3D} \sim 2.5 \cdot 10^{17} \frac{bit}{cm^3}$$



$\sim 10^{11}$ MIPS/cm³

Binary Information Throughput

$N_{tr} = 320$,

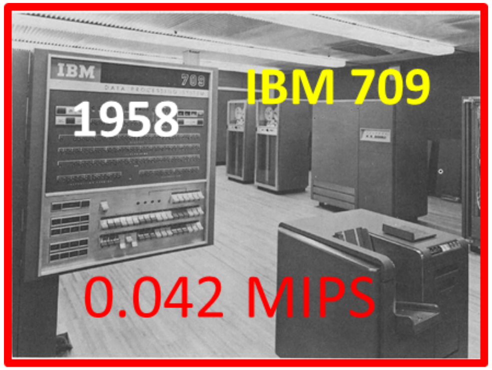
$t_{cycle} \sim 170$ns

$\beta \sim 2\times10^{9}$ bit/s

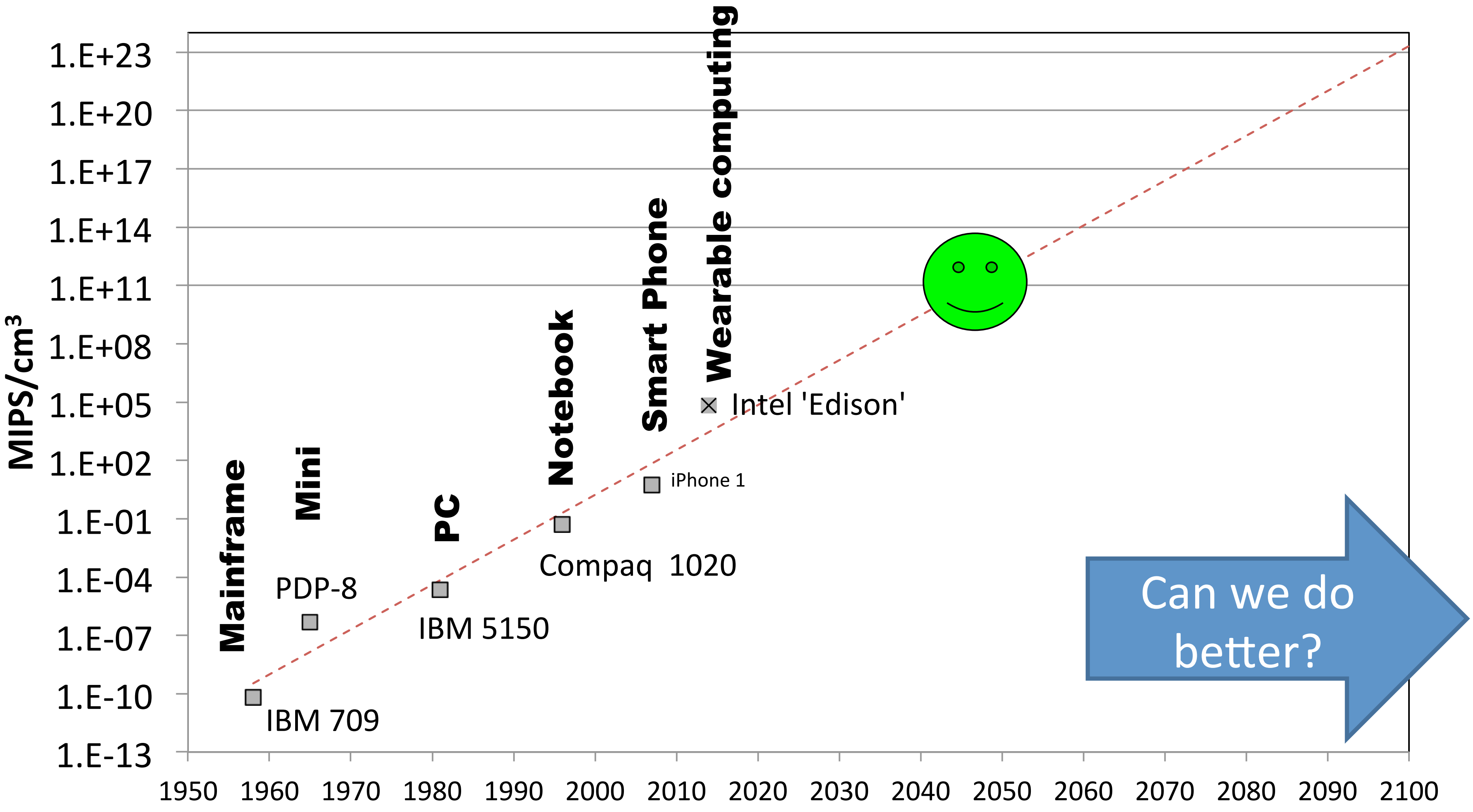
$$\mu = k\beta^{p}$$

Algorithmic performance

$\mu \sim 0.15$ MIPS



System's "intelligence" limit for electron based systems?



Can we do better?

How can we go below 5 nm?

$$\boxed{\mu = k\beta^p} = \frac{n_{bit}}{t_{sw}}$$

Devices having feature sizes less than 5 nm should utilize particles whose mass is greater than the mass of an electron. Below about 5 nm, the mass of information-bearing particle should exceed free electron mass.

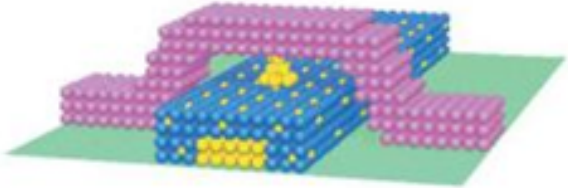
$$L_{\min} = \frac{\hbar}{\sqrt{2mE_b}}$$

Moving atoms instead of moving electrons?

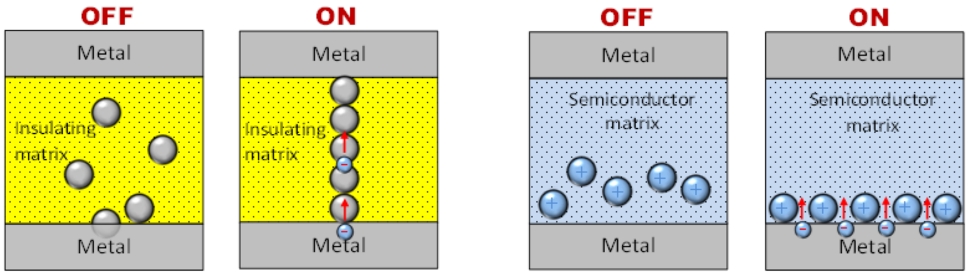
This conclusion resulted from the Heisenberg limit on device size

Moving Atoms: Nanoionics

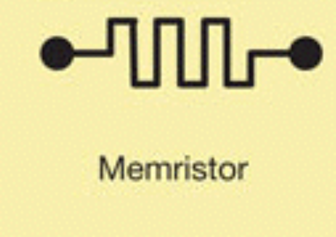
Atomic switch

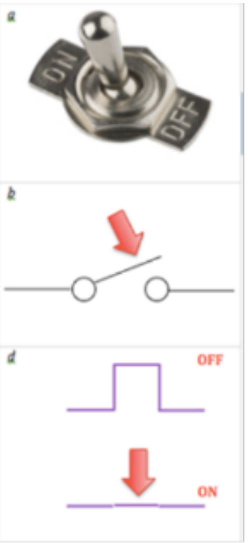


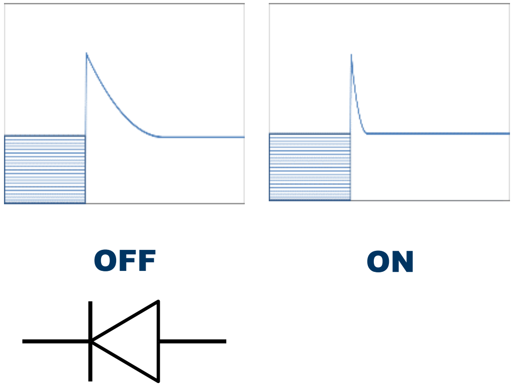
Terabe et al., *Nature* 433, 47-50 (2005)



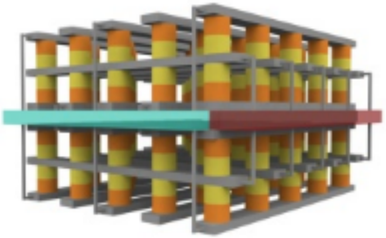
Memristor







Resistive memory



Lee et al. Nature Mater. 10, 625–630 (2011)

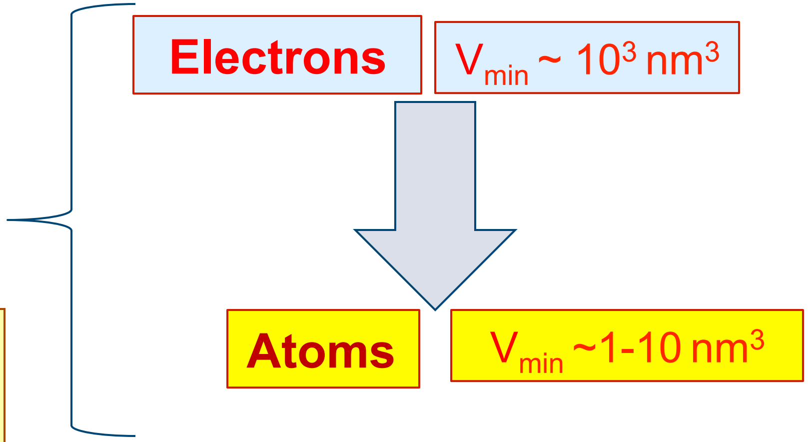
Feature size	
Demonstrated	9 nm

Switching time	
Demonstrated	0.3ns

A SUMMARY: Minimal solid-state binary element

What is the smallest volume of matter needed for a memory cell?

Information carriers



$$a_{\min} = a_H \ln\left(t_r \cdot f_0\right) = \frac{\hbar}{2\sqrt{2mE_b}} \ln\left(t_r \cdot f_0\right)$$

V. V. Zhirnov, R. K. Cavin, S. Menzel, E. Linn, S. Schmelzer, D. Bräuhaus, C. Schindler and R. Waser, "**Memory Devices: Energy-Space-Time Trade-offs**", *Proc. IEEE* 98 (2010) 2185

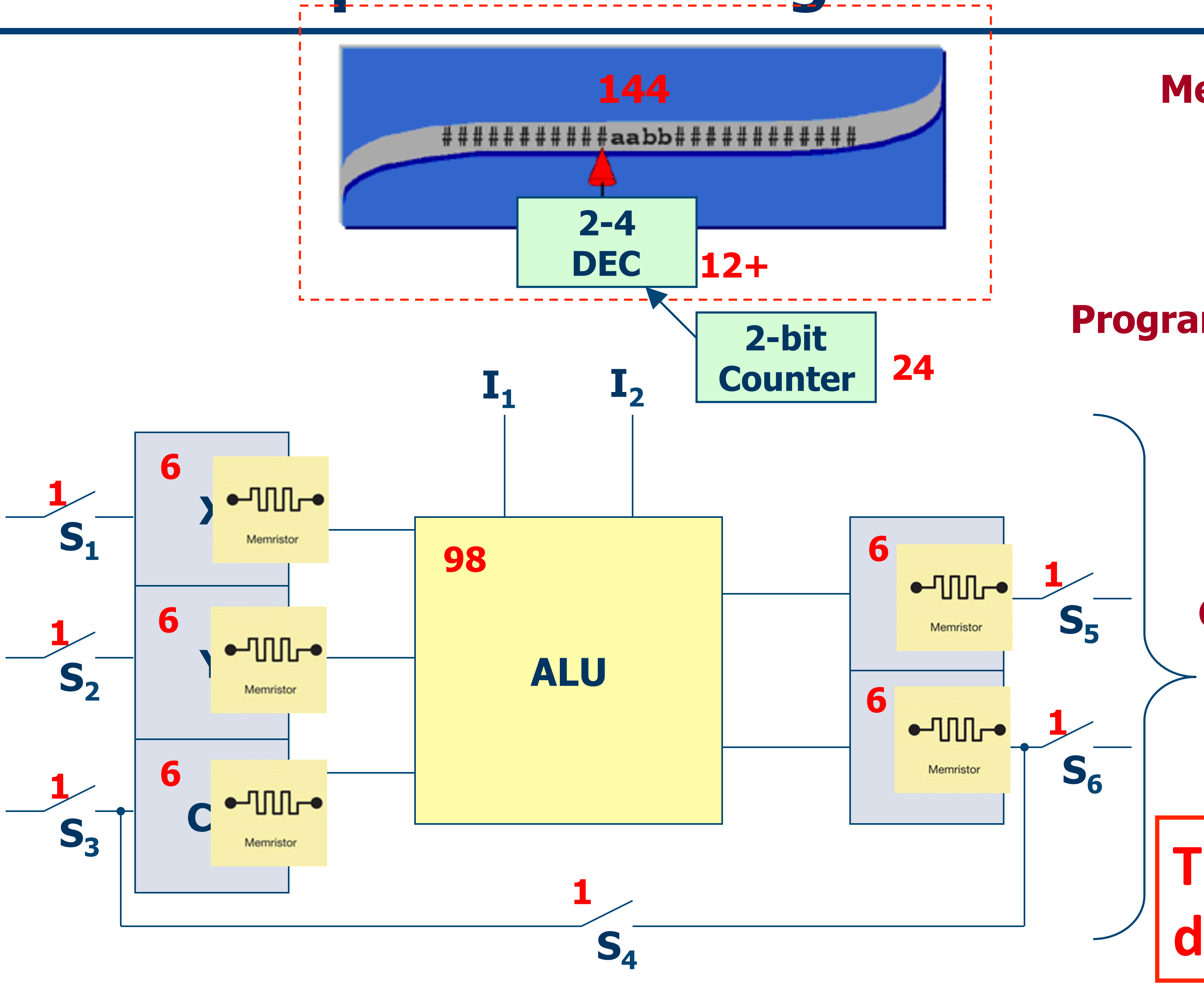
In collaboration with RWTH Aachen Univ / Jülich Res. Ctr.

V. V. Zhirnov, R. Meade, R. K. Cavin, and G. Sandhu, "**Scaling Limits of Resistive Memories**", *Nanotechnology* 22 (2011) 254027

V. V. Zhirnov and G. Sandhu, , "**Scaling limits of nanoionic devices**", in *Resistive Switching*, D. Ielmini, R. Waser, ed., Wiley-VCH, (2014).

In collaboration with Micron Technology, Inc.

Memristor-Based minimal Computational Engine?



Memory

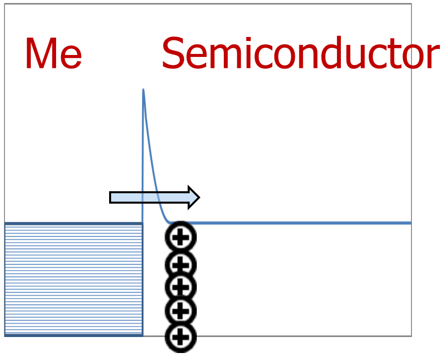
Program Counter

CPU

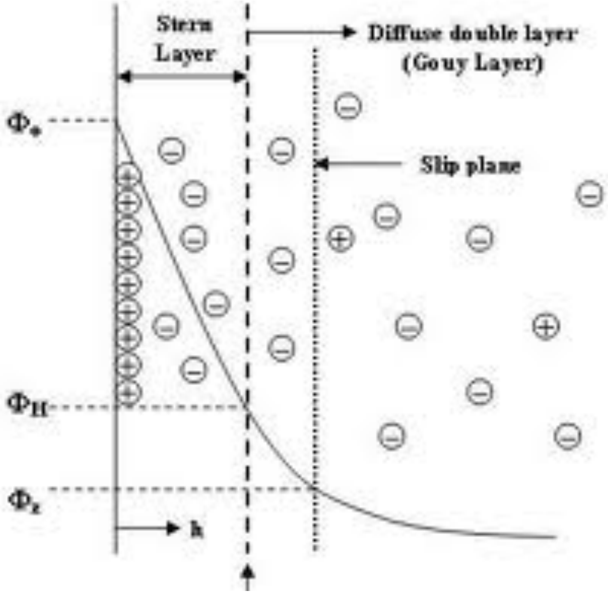
Total: ? devices

Memristors using Liquid Semiconductors' - Electrolytes

The formation of the electrical double-layer at metal-electrolyte interfaces is governed by similar physics as that for the depletion layer metal-semiconductor interfaces



W~5-10nm



W~0.5-1 nm

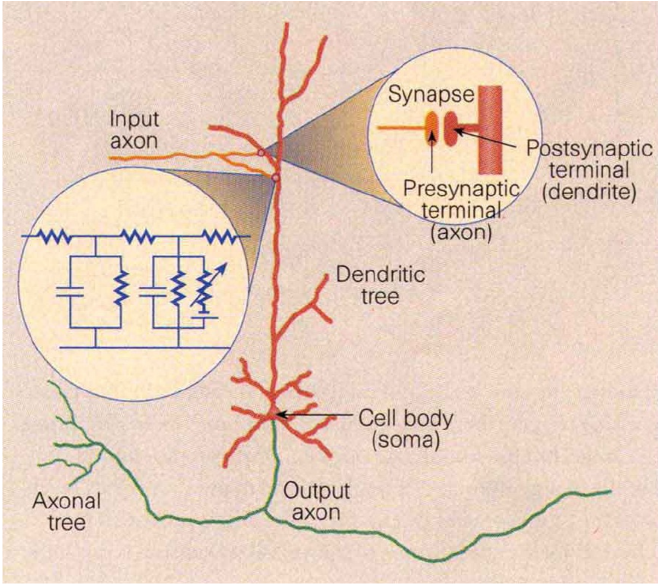
Sub 5nm 'repairable' devices, better heat removal etc.

What next? Ions in liquid electrolytes?

Ions in liquid electrolytes play an important role in biological information processors such as the brain

In the human brain, the distribution of **Ca** ions in dendrites may represent a crucial variable for processing and storing information.

Ca ions enter the dendrites through voltage-gated channels in a membrane, and this leads to rapid local modulations of calcium concentration within dendritic tree



C. Koch, “Computation and single neuron”, Nature 385 (1997) 207

Based on the brain analogy, the binary state can be realized by a single ion that can be moved to one of two defined positions, separated by a membrane (the barrier) with voltage-controlled conductance

Ions are heavy, but brain seems to use them efficiently!

Emerging Technology: Fluid nanoelectonics?

(Stuart Parkin, IBM)

- Fluid nanoelectonics utilizing liquid media may offer a new promising path to replace the foundation of today's computing technologies
  - Why IBM Made a Liquid Transistor - MIT Technology Review, http://www.technologyreview.com/news/512721/why-ibm-made-a-liquid-transistor/
  - NY Times: I.B.M. Research Points to Circuits That Mimic the Brain's Design, http://bits.blogs.nytimes.com/2013/03/21/i-b-m-research-points-to-circuits-that-mimic-the-brains-design/
- Examples include nanoionic devices based on electrolyte-filled nanochannels
  - DNA memory
  - protonic transistors, etc.
- Such structures might be used to make an atom-based binary switch scalable to ~1 nm or below
  - Fluid nanoelectronic systems could be reconfigurable, with individual elements strung together to create wires and circuits that could be reprogrammed
- Although it is at a very early stage, fluid nanoelectronics could someday allow for very powerful and energy-efficient computing

Way Beyond Moore: Information Processing By Nature

1) Living cell as an *in carbo* information processor
2) Information content of a material system/living cell
3) Essential parameters of an *in carbo* processor: Logic and Memory hardware
4) In silico vs. *in carbo* information processors: A comparison

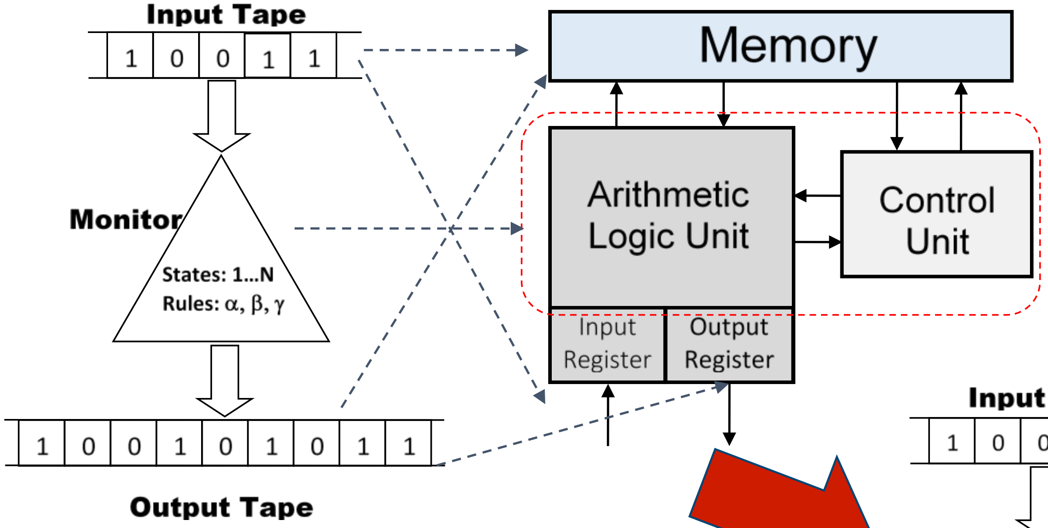
V. V. Zhirnov and R. K. Cavin, "Microsystems for Bioelectronics" (Elsevier 2015)

R. K. Cavin, P. Lugli and V. V. Zhirnov, "Science and Engineering Beyond Moore's Law", *Proc. IEEE* 100 (2012) 1720-1749

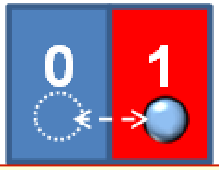
In collaboration with Technische Universität München

Abstract Information Processors

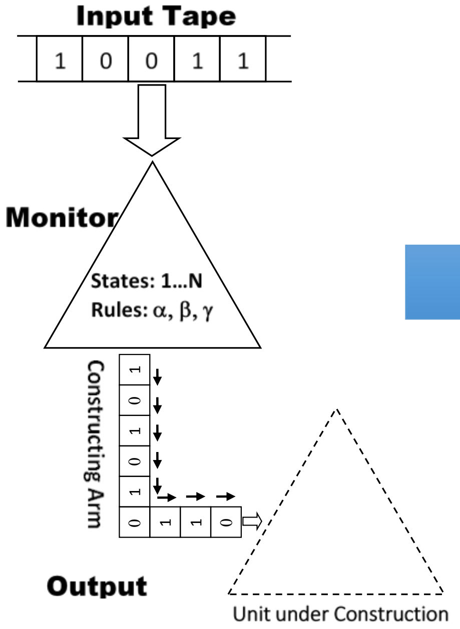
Turing Machine **General-purpose Computer**

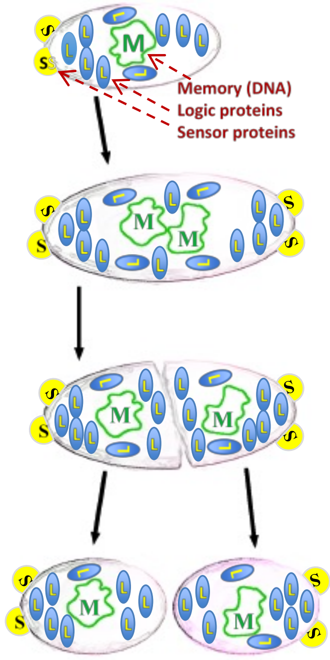


Consider a computer with the task of controlling the assembly of a structure from building blocks



~500 "raw" bit transitions per useful bit



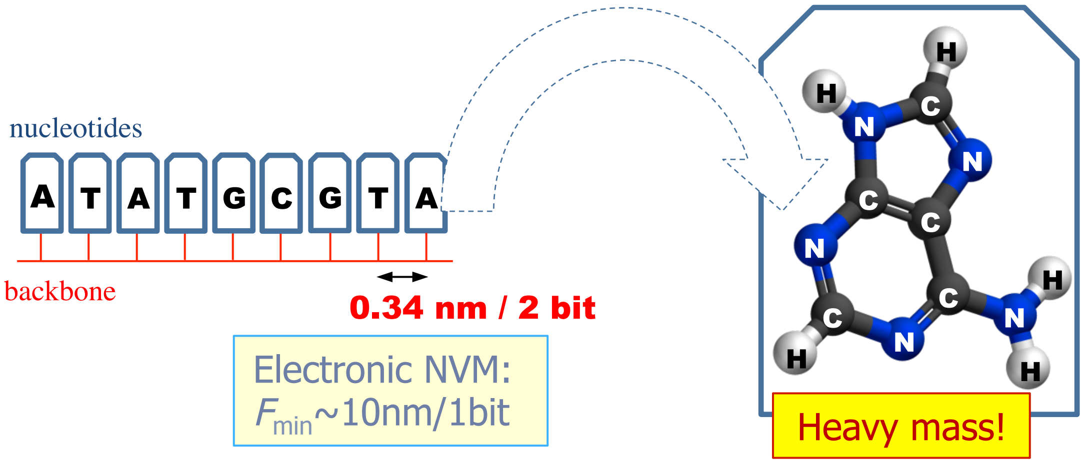


von Neumann Universal Constructor

R. Cavin, W. Joyner, and T. Noll, **Chapter 22**: *Performance Estimates for Microprocessors: at Technology Limits and in Practice*, in: **Nanoelectronics and Information Technology**, by R. Waser (Ed.) (Wiley 2012)

Memory Hardware

- All data about structure and operation of a living cell are stored in the long DNA molecule
  - Nonvolatile memory
- DNA coding uses a **base-4** (quaternary) system
  - The information is encoded digitally by using four different molecular fragments, to represent a state: adenine (A), cytonine (C), guanine (G), and thymine (T).



0.34 nm / 2 bit

Electronic NVM: $F_{\min}$~10nm/1bit

Heavy mass!

$$a_{\min} = \frac{h}{2\sqrt{2mE_b}}$$

DNA is <u>NOT</u> a read-only memory

DNA memory operations

READ

- *Multi-access capability* by distinct computing units

WRITE

Vertical gene transfer - exact copying of the parental DNA

Lateral (horizontal) gene transfer :

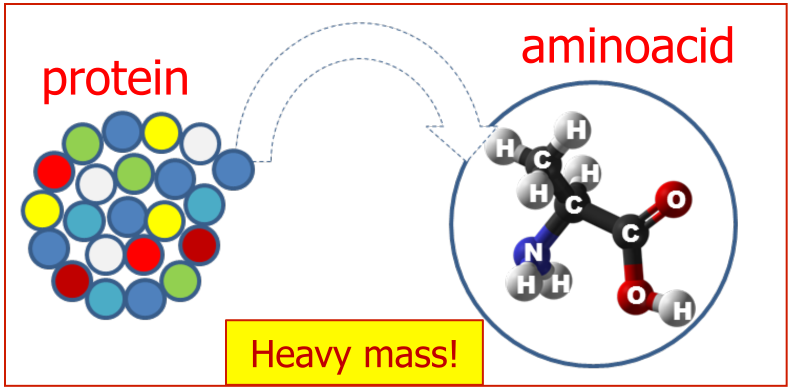
(1) direct uptake ('swallowing') of a naked DNA by a cell,

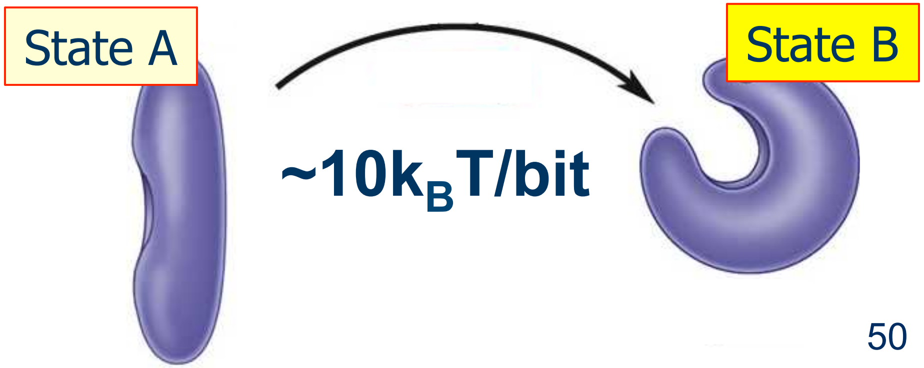
(2) by a virus,

(3) by direct physical contact between two cells.

Logic Hardware

- Many proteins in cells have as their primary function the transfer and processing of information
  - are regarded as logic elements of the in-carbo processor
  - the proportion of components devoted to computational networks increases with the complexity of the cell, and are absolutely dominant in humans
- Proteins can alter their 3D structural shapes (*conformation*) in response to external stimuli,
  - different conformations can represent different logic states.
  - These *nanomechanical* changes form a state variable – **conformon**
  - Different *nanomechanical* conformations of these protein devices are recognized by other elements of the in-carbo cell circuit by a process based on *selective affinity* of certain biomolecules with given conformational states (e.g. electrostatic attraction)





Information Content of Living Cells: An upper bound estimate

Element	% of dry weight	m, kg	N_{at}
C	50	2×10^{-16}	8×10^{9}
O	20	6×10^{-17}	2×10^{9}
N	14	4×10^{-17}	2×10^{9}
H	8	2×10^{-17}	1×10^{10}
P	3	9×10^{-18}	2×10^{8}
S	1	3×10^{-18}	6×10^{7}
K	1	3×10^{-18}	5×10^{7}
Mg	0.5	2×10^{-18}	4×10^{7}
Ca	0.5	2×10^{-18}	2×10^{7}
Fe	0.2	6×10^{-19}	6×10^{6}
Total	98.2%	3×10^{-16}	3×10^{10}

$$I_M = K\left(\log_2 N + 3n\right)$$

$$I_{cell} \sim 3\cdot10^{10}\cdot\left(\log_2 10 + 3\cdot 32\right) \sim 3\cdot10^{12}\,bit$$

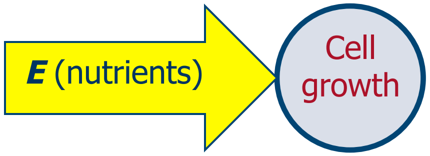
an upper bound on the information content that must be processed to assemble a new cell.

a more accurate estimate: $\langle I\rangle = \sum_i^N p_i I_i(p_i) = \sum_i^N -Cp_i \log p_i = -C\sum_i^N p_i \log p_i$

Information Content of Bacterial Cells: Theory vs. Experimental Estimates

- An upper bound estimate: ~3×10^{12} bits (this work)
- Experimental estimates: 10^{11}-10^{13} bits
  - Experimental estimates of the information content of living cells were made based on *microcalorimetric measurements*.
  - It has been concluded that the major consumption of energy during a cell's reproduction cycle arises from the correct placement of molecules within the cell.

W. W. Forrest, "*Entropy of microbial growth*", *Nature* 225 (1970) 1165-1166



$$\Delta E = T\Delta S + P\Delta V + \sum_i \mu_i \Delta N_i$$

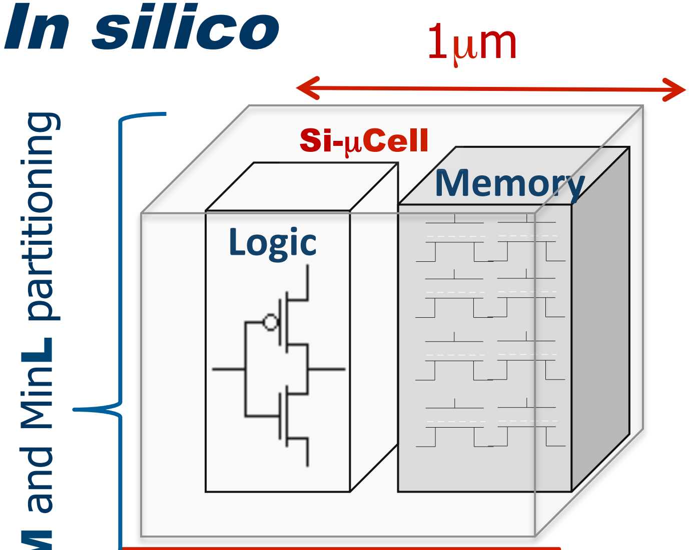
$\Delta I = -\Delta S$

- In the following, the conservative edge of the estimated range is used: ~10^{11} bits
  - (the number of *output bits*)

Raw bits processed per output bit

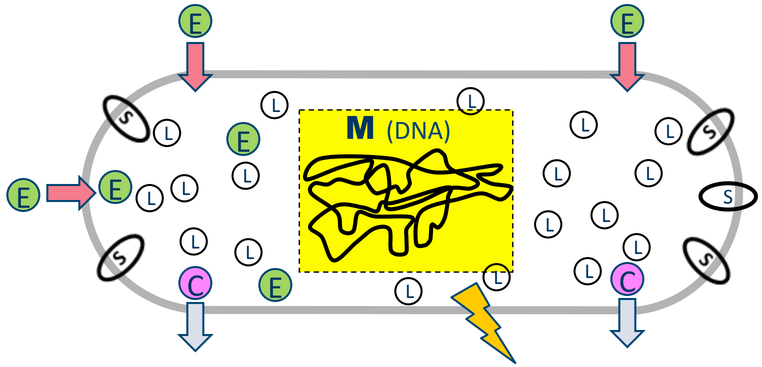
In-Carbo system specs

In silico



Memory: 250 kbit
Logic: 320 bit

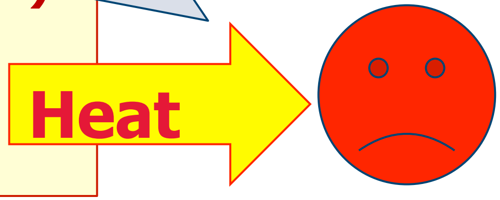
In carbo



Computational Task: **10^{11} output bits**
Task Time: **2400s**

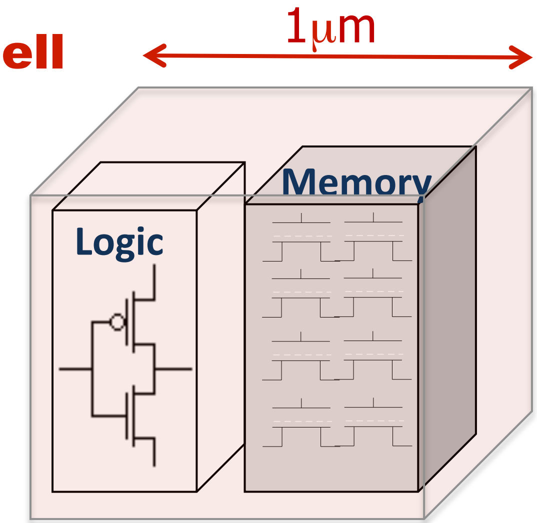
Matching the bio-µCell

Computational Task: **10^{11} output bits**
(~5×10^{13} raw bits)
Task Time: **2400 s**
Cycles per output bit: **3**
Required cycle time: **8 ns**



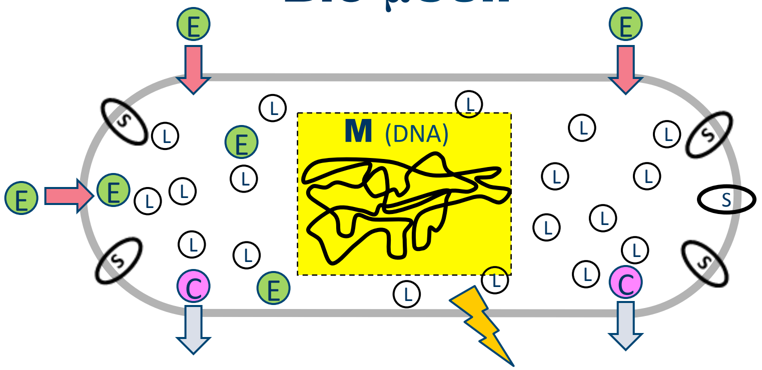
In-Silico versus *In-Carbo*

Si-µCell



Memory:	~10^5bit
Logic:	~300–100,000 bit
Power:	~10^{-7} W
Heat:	~1 W/cm^2
Total energy/task*:	**~10^{-3} J**
Task time*:	50,000 s ~ 14h

Bio-µCell



Memory:	10^7 bit
Logic:	>10^6 bit
Power:	10^{-13} W
Heat:	10^{-6} W/cm^2
Total energy/task*:	**10^{-9} J**
Task time*:	2400s=40min

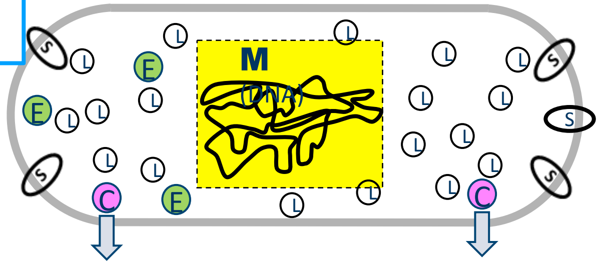
*Equivalent to 10^{11} output bits

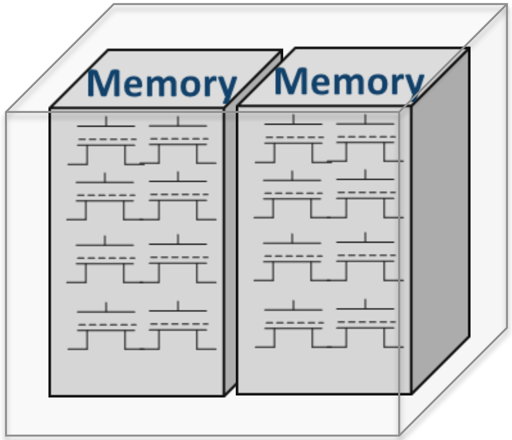
A Si-µCell fundamentally cannot match the bio-µCell in the operational energy.

DNA Memory µSystem

Given:
Memory: 9.6 Mbit
Power: 10^{-13} W
Task time*: 2400s=40min

~10Mbit





N~ 100 kbit
$E \sim 10^{-14}$ J

Simplifying Assumption:

The entire DNA information content is read and written at least once during one cell division cycle

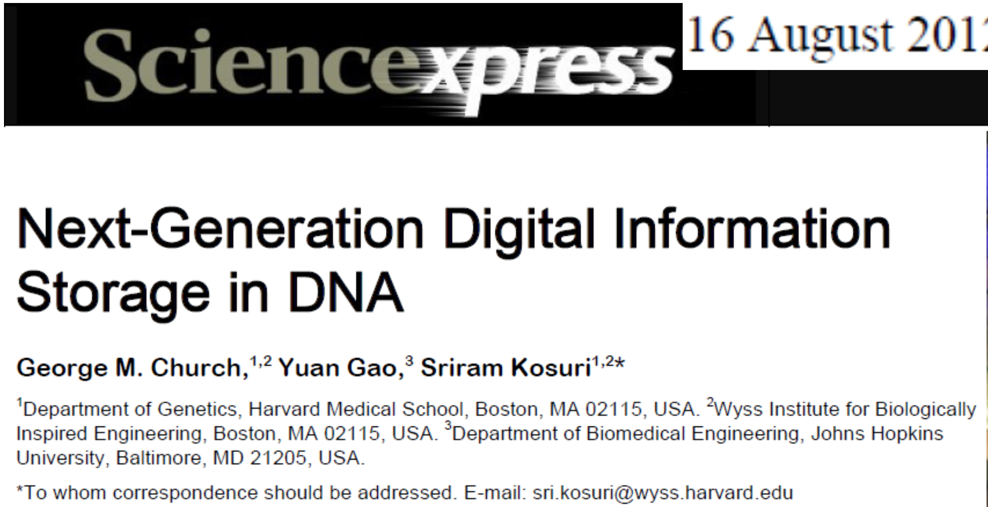
Characteristic access time per bit:

$$t_{bit} \sim \frac{2400}{2\cdot 9.6\cdot 10^{6}} \sim 100\,\mu s$$

Characteristic energy per bit (system-level):

$$E < \frac{10^{-13}\,W\cdot 2400s}{2\cdot 9.6\cdot 10^{6}} = 2.5\cdot 10^{-17}\,\frac{J}{bit}$$

Example I: DNA Memory



Sciencexpress 16 August 2012

Next-Generation Digital Information Storage in DNA

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http://www.wired.com/wiredscience/2012/08/dna-data-storage/

DNA: The Ultimate Hard Drive?

Researchers **stored an entire genetics textbook** in less than a picogram of DNA — one trillionth of a gram — an advance that could revolutionize our ability to save data.

5.27×10^6 bit

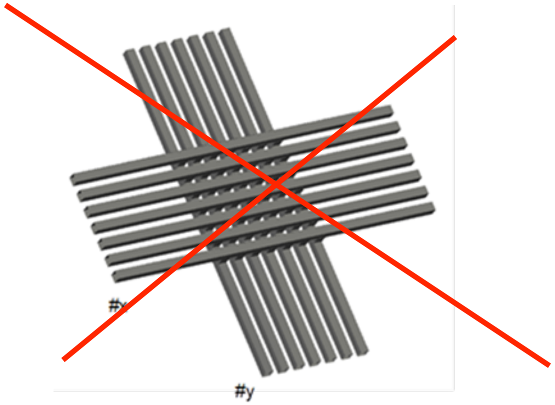
DNA memory can be stable ~ 100y+

HARDWARE: Agilent Oligo Library Synthesis microarray platform

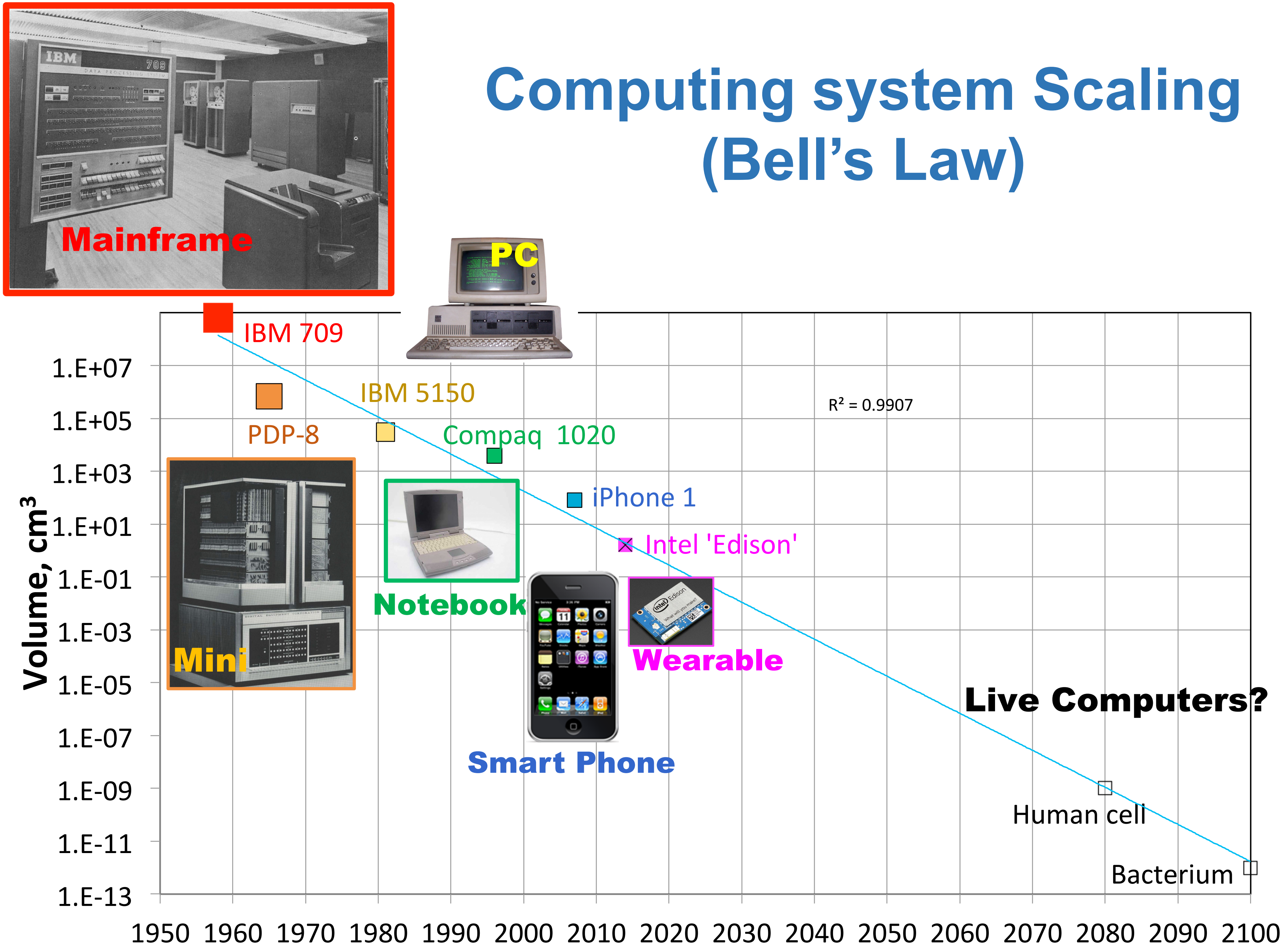
- Agilent Technologies, a spin-off of Hewlett-Packard (1999), originally a semiconductor company, which became now a global company offering products & services in communications, electronics, semiconductor, test and measurement, life sciences and chemical analysis industries.
  - Example of a successful convergence of semiconductor and bio industries

Design Secrets of ***in carbo*** system

- Heavier mass of information carrier
  - Molecules instead electrons
  - Smaller device size
- Array-less memory organization
  - energy minimization
- Utilized ambient thermal energy
  - For *in silico* systems thermal energy is an enemy!
- Flexible/on-demand connections/routing
  - *In silico*: most energy is consumed by interconnect



Computing system Scaling (Bell’s Law)



Conclusions

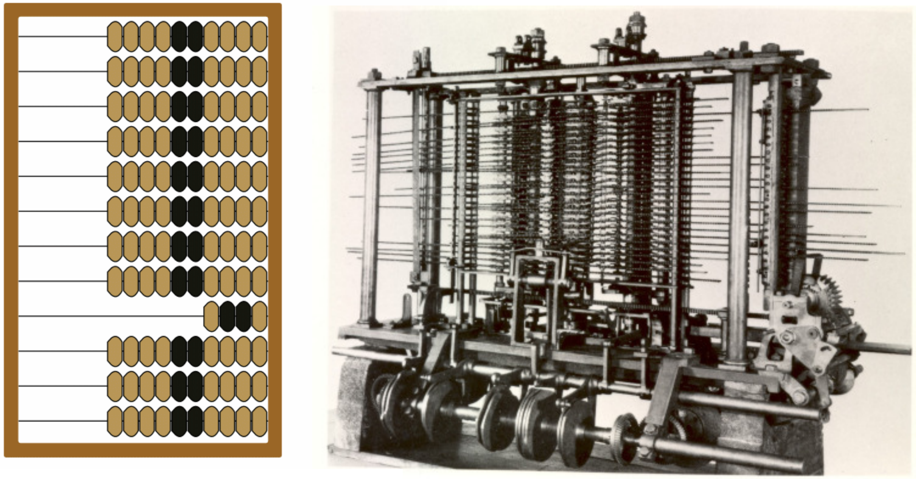
- Basic physics enables key insights into the limits of component and system scaling

- Extreme component scaling holds the promise of highly functional micron-scale systems

- Micron-scale energy sources are key to extreme microsystems
  - Design space is bounded by the limits of energy sources
- Communication energy/volume expenditures is most costly activity – should therefore maximize "system intelligence"

- We suggest that inspiration for future ultra-low energy computing architectures can be derived from organic systems, i.e., at the intersection of chemistry, biology, and information processing

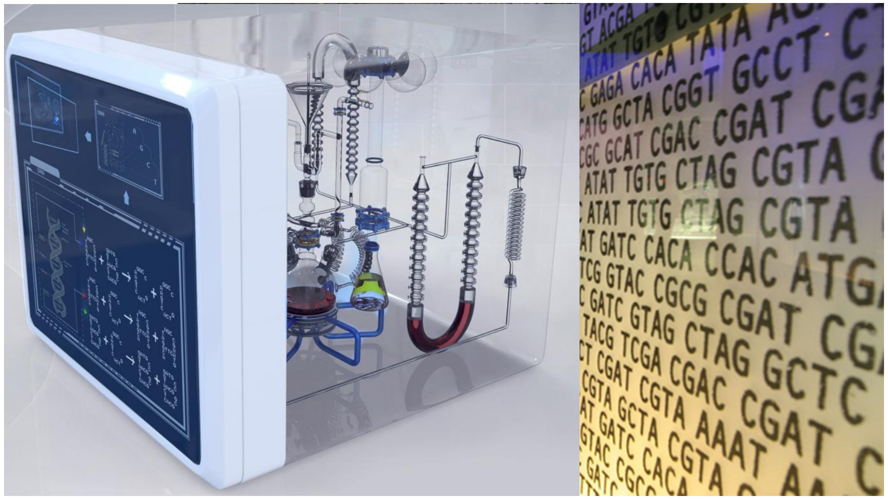
Do all computing engines have a common soul?



Mechanical

Electrical

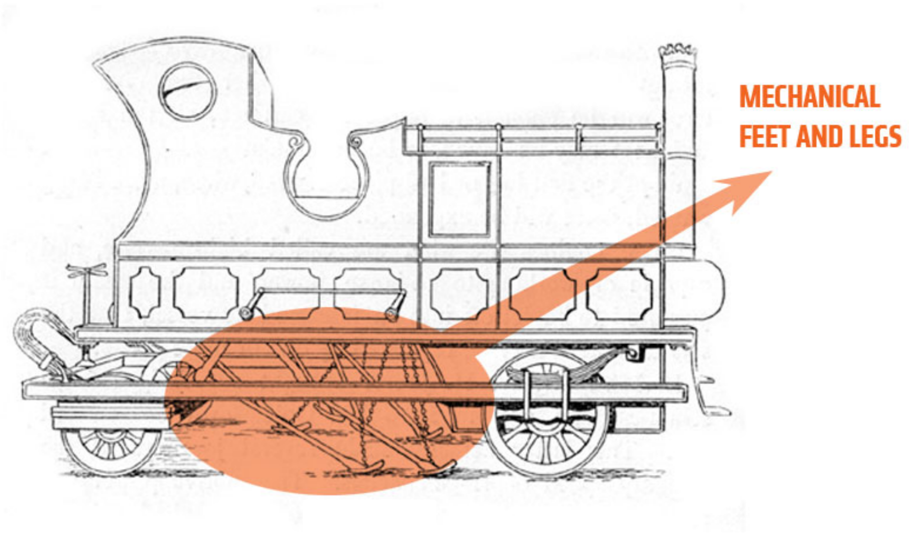
Chemical???



Yan Liang, L2XY2.com/UW News

An Early Steam Car Used Mechanical Feet To Move

In 1824, David Gordon designed and built a three-wheeled, *six-legged* steam carriage.



He emulated a mode of transportation he knew worked very well horses

MIPS as an indicator of hardware performance

P. Hilbert and M. Lopez, "The world's technological capacity to store, communicate and compute information", Science 332 (2011) 60

- Measuring the computational power of digital devices is not an easy task
  - Their characteristics are multidimensional

- The final choice of our unit of measurements was determined principally by the availability of relevant and consistent statistics, <u>more than their robustness</u>

- Dhrystone VAX MIPS as units of measurements
  - Extensive databases available
  - Conversion from SPEC to Dhrystone MIPS established
  - Conversion from FLOPS to Dhrystone MIPS established

System Constraint on Minimum Energy per Bit

$$\Pi_{syst} = \left(1-\Pi_{err}\right)^{N}$$

The probability that all N switches in a circuit work correctly

$$\Pi_{syst} > \Pi_{crit}$$

e.g., → 0.5 lower boundary

e.g., → 0.99 a “reasonable” boundary

$$\Pi_{err} = 1-\Pi_{crit}^{\frac{1}{N}}$$

$$\Pi_{err} = f(E_b)$$

$$\boxed{E_{b_{\min}} = f(N)}$$

$$\boxed{N_{\max} \sim \frac{1}{a^2}}$$

$$\Pi_{err} = \overset{\text{Boltzmann}}{\boxed{\exp\left(-\frac{E_b}{kT}\right)}} + \overset{\text{Heisenberg}}{\boxed{\exp\left(-\frac{2\sqrt{2m}}{\hbar}a\sqrt{E_b}\right)-\exp\left(-\frac{\hbar E_b+2akT\sqrt{2mE_b}}{\hbar kT}\right)}}$$

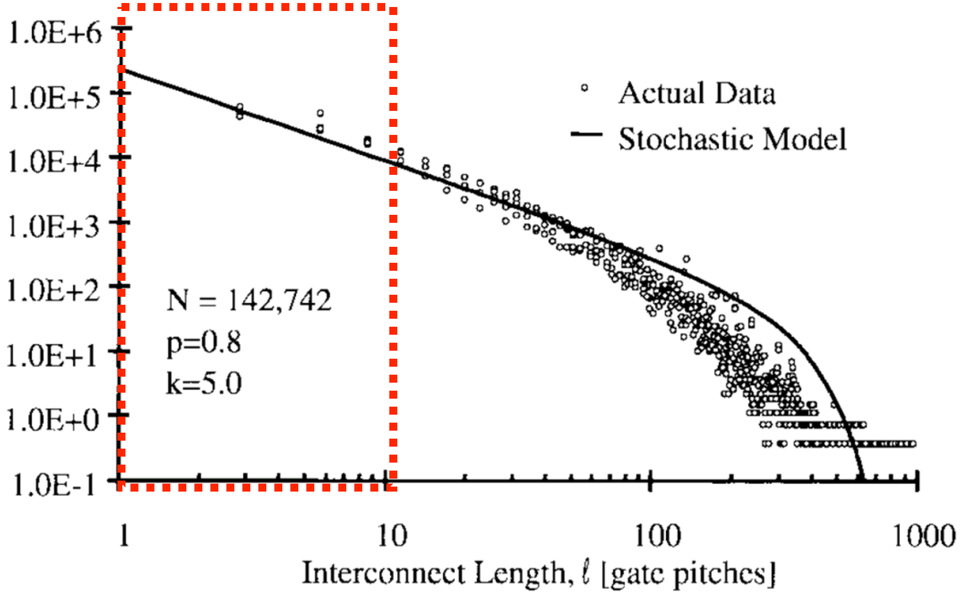
Long Interconnects

- In interconnects, the number of electrons needs to be sufficient to guarantee successful communication between binary switches

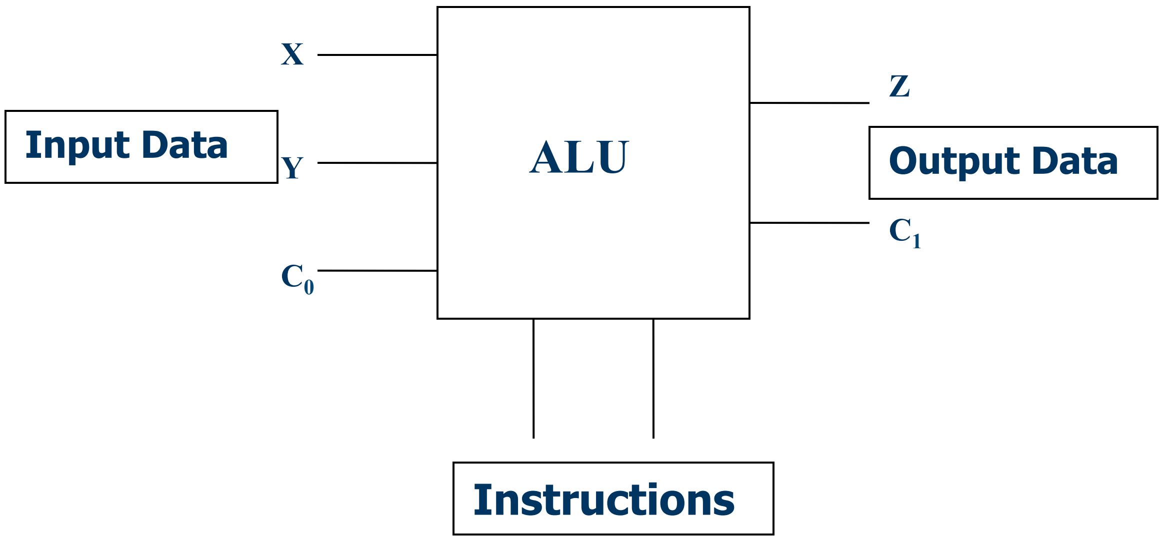
n=2 **L=100a**

$$\Pi_n = \left(1-\left(1-\frac{a}{L}\right)^N\right)^n$$

N electrons	Operational reliability	
121	50%	**E~120k_BT**
198	75%	**E~200k_BT**
487	99%	**E~500k_BT**



1-bit ALU example – simple Turing Machine model



The minimal ALU does 2^2=4 operations on two 1-bit X and Y:
Operation 1: X AND Y
Operation 2: X OR Y
Operation 3: (X+Y)
Operation 4: (X+(NOT Y))

Supports functionally complete set of logic and arithmetic operations